ML (4606)
PH (4564)
PITNEY, HARDIN, KIPP & SZUCH LLP
(MAIL TO) P.O. BOX 1945, MORRISTOWN, N.J. 07962-1945
(DELIVERY TO) 200 CAMPUS DRIVE, FLORHAM PARK, N.J. 07932-0950
(973) 966-6300

ATTORNEYS FOR Plaintiff
Matsushita Electric Industrial Co., Ltd.

UNITED STATES DISTRICT COURT
DISTRICT OF NEW JERSEY

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.,	:	
Plaintiff,	:	Civil Action No. 02-336 (WGB)
v.	:	COMPLAINT
SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC. and SAMSUNG AUSTIN SEMICONDUCTOR, L.L.C.,	:	
Defendants.	:	

Plaintiff Matsushita Electric Industrial Co., Ltd. ("MEI"), by and through its attorneys, complain of defendants Samsung Electronics Co., Ltd. ("SEI"), Samsung Electronics America, Inc. ("SEA"), Samsung Semiconductor, Inc. ("SSI") and

Samsung Austin Semiconductor, L.L.C. ("SAS") (collectively "Defendants") as follows:

Jurisdiction And Venue

1. This is an action for patent infringement which arises under the Patent Laws of the United States, including Title 35, United States Code, Sections 271 and 281 through 285. This Court has subject matter jurisdiction pursuant to Title 28, United States Code, Sections 1331 and 1338(a).

2. Venue properly lies in this Judicial District pursuant to Title 28, United States Code, Sections 1391(b), (c) and 1400(b) because Defendants are deemed to reside in this State and/or have committed acts of infringement and/or have a regular and established place of business in this Judicial District.

3. Defendants are subject to the personal jurisdiction of this Court by virtue of their contacts with the State of New Jersey and/or by virtue of making, using, selling, offering for sale and/or importing in this Judicial District and elsewhere in the United States devices that embody the inventions disclosed and claimed in the patents in suit.

The Parties

4. Plaintiff MEI is a corporation organized and existing under the laws of Japan, having an office and place of business at 1006 Kadoma, Kadoma City, Osaka 571-8501, Japan.

5. Upon information and belief, defendant SEI is a corporation organized and existing under the laws of the Republic of Korea, having an office and place of business at 416 Maetan 3-Dong, Paldal-Ku, Suwon, Kyonggi, Republic of Korea. Upon information and belief, SEI conducts business in this Judicial District through its wholly owned subsidiary, SEA, at 105 Challenger Road, Ridgefield Park, New Jersey 07660.

6. Upon information and belief, defendant SEA is a corporation organized and existing under the laws of the State of New York, having an office and place of business at 105 Challenger Road, Ridgefield Park, New Jersey 07660.

7. Upon information and belief, defendant SSI is a corporation organized and existing under the laws of the State of California, having an office and place of business at 3655 N. 1st Street, San Jose, California 95134.

8. Upon information and belief, defendant SAS is a corporation organized and existing under the laws of the State of Texas, having an office and place of business at 12100 Samsung Blvd., Austin, Texas 76754.

COUNT I

INFRINGEMENT OF U.S. PATENT NO. 5,375,095

9. MEI realleges and incorporates herein by reference the allegations of Paragraphs 1-8 of this Complaint.

10. On December 20, 1994, United States Letters Patent No. 5,375,095 ("the '095 Patent") entitled "Semiconductor Memory Apparatus With Reduced Line Widths" was duly and legally issued. A copy of the '095 Patent is attached hereto as Exhibit 1.

11. MEI is the assignee and owner of all right, title and interest in and to the '095 Patent. Accordingly, MEI has the right to bring this suit for damages and injunctive relief.

12. Upon information and belief, Defendants have been and are currently infringing, in violation of 35 U.S.C. § 271, one or more claims of the '095 Patent by making, using, selling, offering for sale and/or importing in this Judicial District and elsewhere in the United States devices that embody the inventions disclosed and claimed in the '095 Patent, including, but not limited to, synchronous dynamic random access memory devices.

13. Upon information and belief, the acts of Defendants alleged herein have been and continue to be willful, deliberate and intentional.

14. The acts of Defendants alleged herein have been and continue to be performed without the permission, license, or consent of MEI.

15. Defendants' infringement of the '095 Patent has injured and damaged MEI and will cause MEI additional injury and

damage in the future unless Defendants are enjoined from infringing the '095 Patent.

16. Damage as a result of the acts of Defendants as aforesaid, are in an amount thus far not yet determined or ascertained, but presently believed to be in excess of One Hundred Million Dollars ($100,000,000).

COUNT II

INFRINGEMENT OF U.S. PATENT NO. 5,053,998

17. MEI realleges and incorporates herein by reference the allegations of Paragraphs 1-8 of this Complaint.

18. On October 1, 1991, United States Letters Patent No. 5,053,998 ("the '998 Patent") entitled "Semiconductor Memory Device With Dual Drivers To Sense Amp Array" was duly and legally issued. A copy of the '998 Patent is attached hereto as Exhibit 2.

19. MEI is the assignee and owner of all right, title and interest in and to the '998 Patent. Accordingly, MEI has the right to bring this suit for damages and injunctive relief.

20. Upon information and belief, Defendants have been and are currently infringing, in violation of 35 U.S.C. § 271, one or more claims of the '998 Patent by making, using, selling, offering for sale and/or importing in this Judicial District and elsewhere in the United States devices that embody the inventions disclosed and claimed in the '998 Patent, including,

but not limited to, synchronous dynamic random access memory devices.

21. Upon information and belief, the acts of Defendants alleged herein have been and continue to be willful, deliberate and intentional.

22. The acts of Defendants alleged herein have been and continue to be performed without the permission, license, or consent of MEI.

23. Defendants' infringement of the '998 Patent has injured and damaged MEI and will cause MEI additional injury and damage in the future unless Defendants are enjoined from infringing the '998 Patent.

24. Damage as a result of the acts of Defendants as aforesaid, are in an amount thus far not yet determined or ascertained, but presently believed to be in excess of One Hundred Million Dollars ($100,000,000).

COUNT III

INFRINGEMENT OF U.S. PATENT NO. 5,475,648

25. MEI realleges and incorporates herein by reference the allegations of Paragraphs 1-8 of this Complaint.

26. On December 12, 1995, United States Letters Patent No. 5,475,648 ("the '648 Patent") entitled "Redundancy Semiconductor Memory Device Which Utilizes Spare Memory Cells From A Plurality of Different Memory Blocs, And Utilizes The Same Decode Lines

For Both The Primary And Spare Memory Cells" was duly and legally issued. A copy of the '648 Patent is attached hereto as Exhibit 3.

27. MEI is the assignee and owner of all right, title and interest in and to the '648 Patent. Accordingly, MEI has the right to bring this suit for damages and injunctive relief.

28. Upon information and belief, Defendants have been and are currently infringing, in violation of 35 U.S.C. § 271, one or more claims of the '648 Patent by making, using, selling, offering for sale and/or importing in this Judicial District and elsewhere in the United States devices that embody the inventions disclosed and claimed in the '648 Patent, including, but not limited to, synchronous dynamic random access memory devices.

29. Upon information and belief, the acts of Defendants alleged herein have been and continue to be willful, deliberate and intentional.

30. The acts of Defendants alleged herein have been and continue to be performed without the permission, license, or consent of MEI.

31. Defendants' infringement of the '648 Patent has injured and damaged MEI and will cause MEI additional injury and damage in the future unless Defendants are enjoined from infringing the '648 Patent.

32. Damage as a result of the acts of Defendants as aforesaid, are in an amount thus far not yet determined or ascertained, but presently believed to be in excess of One Hundred Million Dollars ($100,000,000).

Prayer For Relief

WHEREFORE, Plaintiff MEI prays for judgment that:

a. Defendants have infringed the '095, '998, and '648 Patents.

b. Defendants and their respective agents, servants, officers, directors, employees and all persons acting in concert with defendants directly or indirectly, be permanently enjoined from infringing, inducing others to infringe or contributing to the infringement the '095, '998, and '648 Patents;

c. Defendants be ordered to account for and pay to MEI the damages to which MEI is entitled as a consequence of the infringements;

d. Such damages be trebled for the willful, deliberate and intentional infringements by Defendants as alleged herein.

e. MEI be awarded prejudgment interest, and its costs, disbursements and attorneys' fees herein in accordance with Title 35 United States Code § 285; and

f. MEI be awarded such other and further relief as the Court may deem just and proper under the circumstances.

Respectfully submitted,

PITNEY, HARDIN, KIPP & SZUCH LLP
Attorneys for Plaintiff

By: _____
PAUL J. HALASZ
Counsel to the Firm

Dated: January 25, 2002

OF COUNSEL:
Morton Amster
Abraham Kasdan
Michael V. Solomita
AMSTER, ROTHSTEIN & EBENSTEIN
90 Park Avenue
New York, New York 10016
(212) 697-5995

CERTIFICATION PURSUANT TO LOCAL CIV. R. 11.2

The undersigned hereby certifies that the within matter in controversy is not the subject of any other action pending in any court or of any pending arbitration or administrative proceeding.

PAUL J. HALASZ

January 25, 2002

EXHIBIT 1

US005375095A

United States Patent [19]

Yamada et al.

[11] Patent Number: 5,375,095

[45] Date of Patent: Dec. 20, 1994

[54] SEMICONDUCTOR MEMORY APPARATUS WITH REDUCED LINE WIDTHS

[75] Inventors: Toshio Yamada, Osaka; Michihiro Inoue, Ikoma; Junko Hasegawa, Osaka, all of Japan

[73] Assignee: Matsushita Electric Industrial Co., Ltd., Japan

[21] Appl. No.: 713,500

[22] Filed: Jun. 12, 1991

[30] Foreign Application Priority Data

Jul. 6, 1990 [JP] Japan 2-179835
Jan. 28, 1991 [JP] Japan 3-8713

[51] Int. Cl.[5] G11C 8/00; G11C 7/00
[52] U.S. Cl. 365/230.03; 365/230.06; 365/226; 365/189.09; 365/196; 327/51
[58] Field of Search 365/230.03, 182, 205, 365/226, 530, 227, 228, 229, 189.09, 196, 208, 214, 230.06

[56] References Cited

U.S. PATENT DOCUMENTS

4,761,371	8/1988	Golke et al.	365/205
4,980,799	12/1990	Tobita	365/182
5,040,144	8/1991	Pelley et al.	365/226
5,072,425	12/1991	Kohno et al.	365/226
5,231,607	7/1993	Yoshida et al.	365/226

Primary Examiner—Timothy P. Callahan
Assistant Examiner—Trong Phan
Attorney, Agent, or Firm—Parkhurst, Wendel & Rossi

[57] ABSTRACT

A dynamic random access memory is formed with two power supply meshes extending throughout a memory array region in which are formed memory cells and sense amplifier circuits, thereby enabling sense amplifier drive circuits to be distributed throughout that memory array region, with each sense amplifier drive circuit being connected to the nearest points on the two supply meshes. A substantially improved value of read access time, or increased total memory capacity, can thereby be achieved by comparison with a DRAM in which the sense amplifier drive circuits are provided only at the periphery of a memory array region.

9 Claims, 15 Drawing Sheets

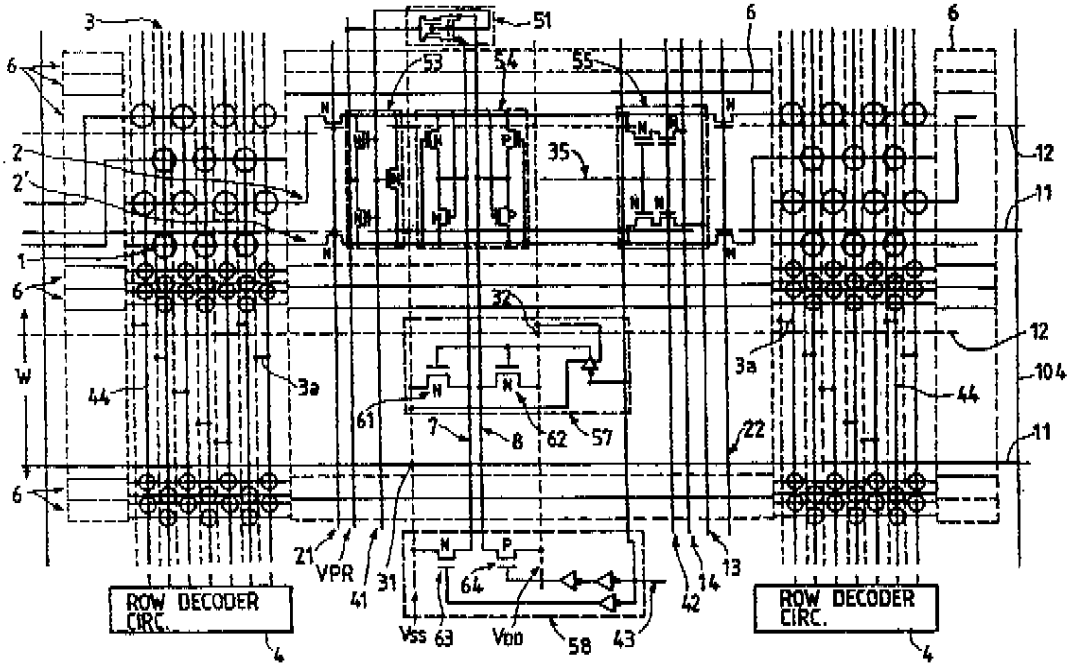


FIG. 1A
(prior art)

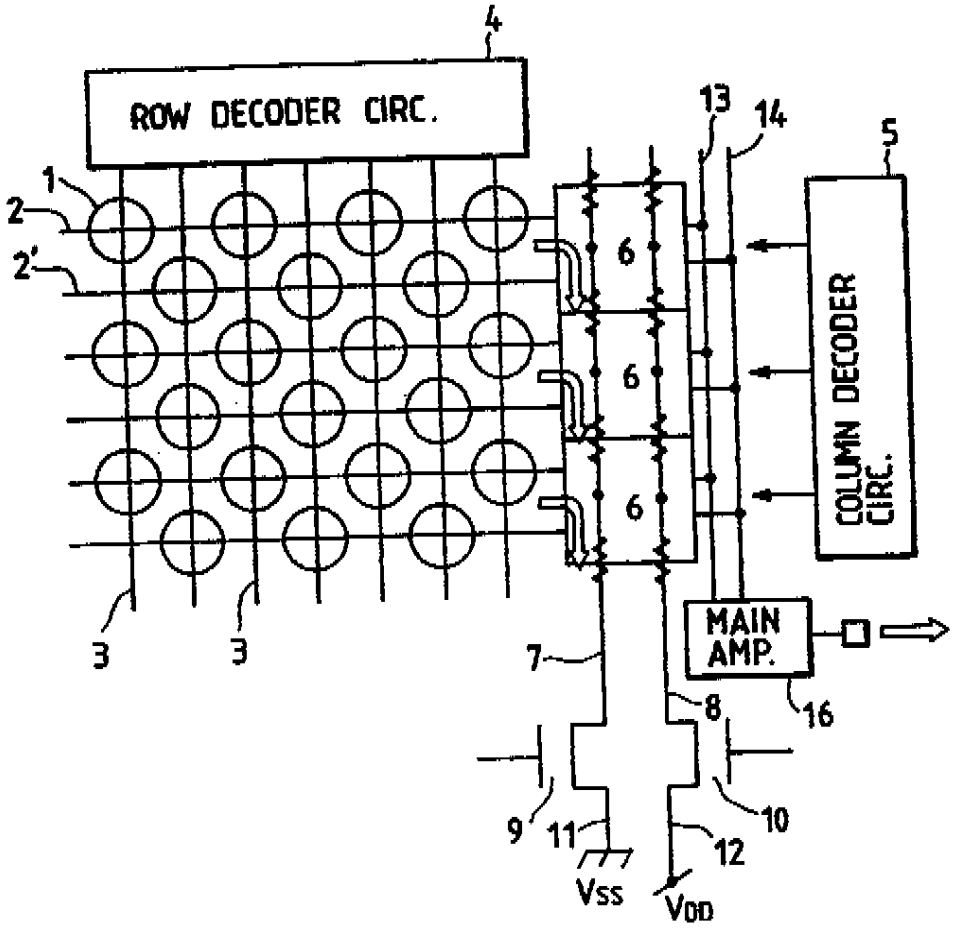


FIG. 1B
(prior art)

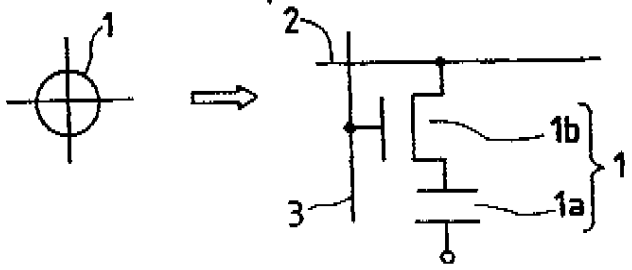


FIG. 2
(prior art)

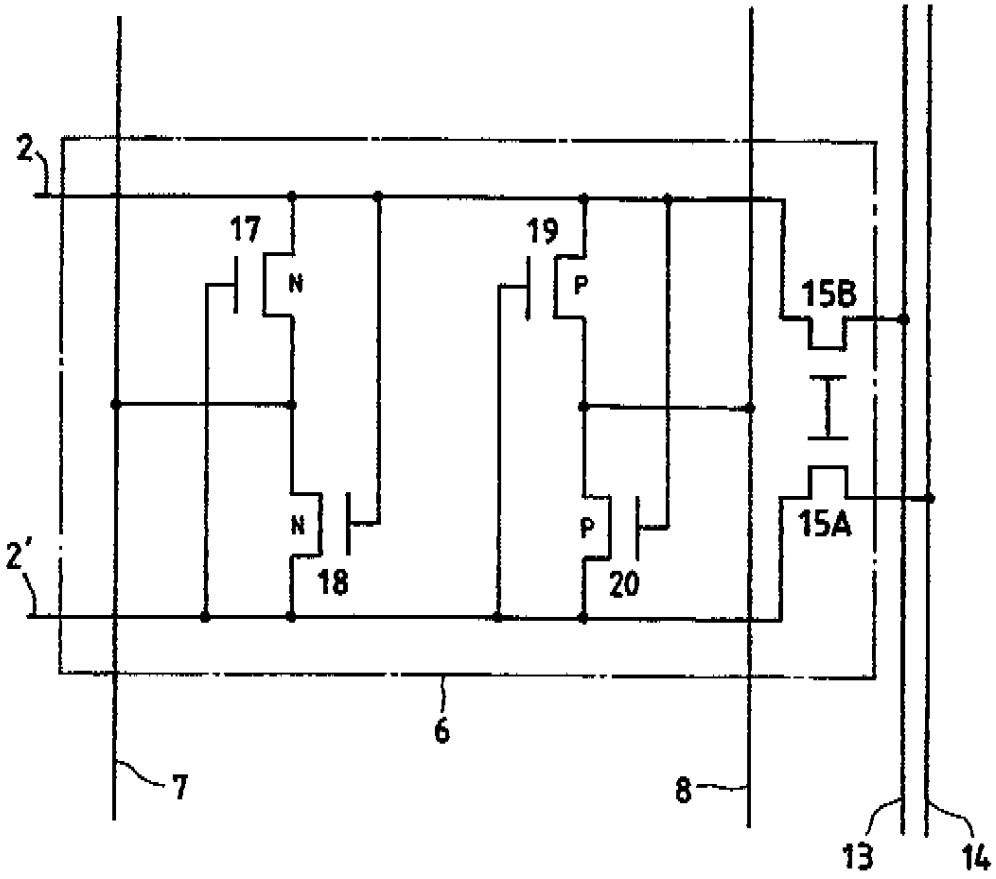


FIG. 3

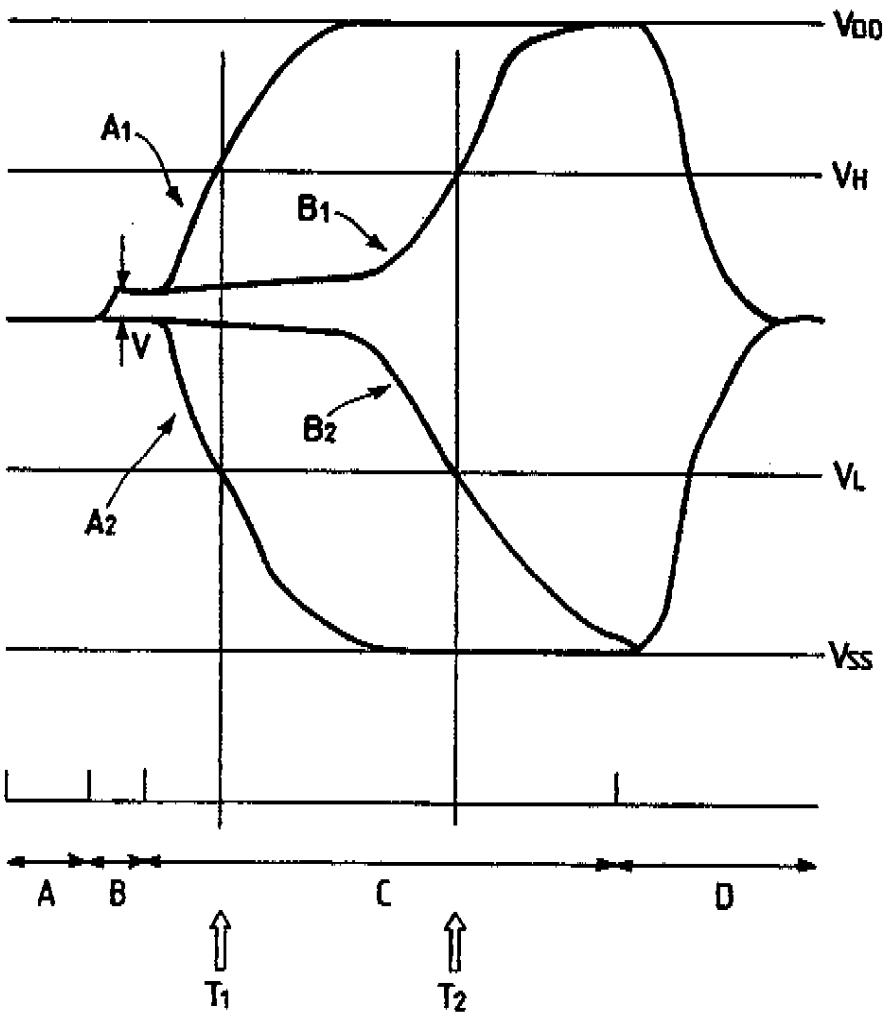


FIG. 4

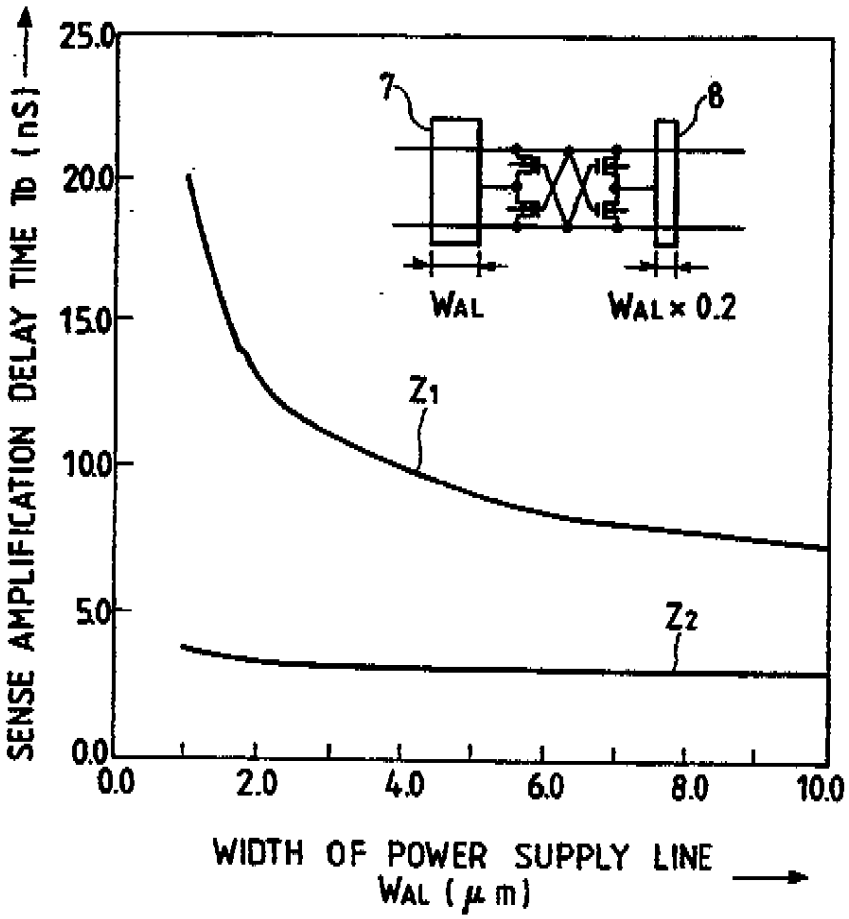

SENSE AMPLIFICATION DELAY TIME Td (nS)
25.0
20.0
15.0
10.0
5.0
0.0
0.0
2.0
4.0
6.0
8.0
10.0
WIDTH OF POWER SUPPLY LINE
WAL (μm)
7
8
WAL
WAL × 0.2
Z1
Z2

FIG. 5A

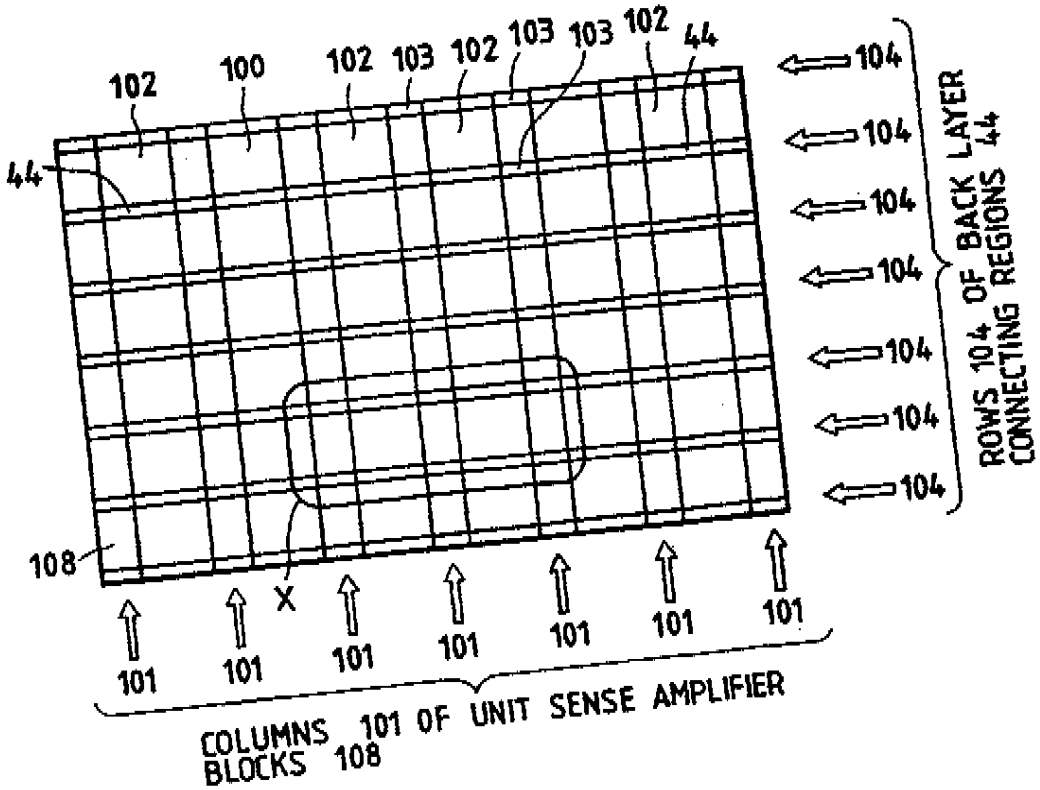
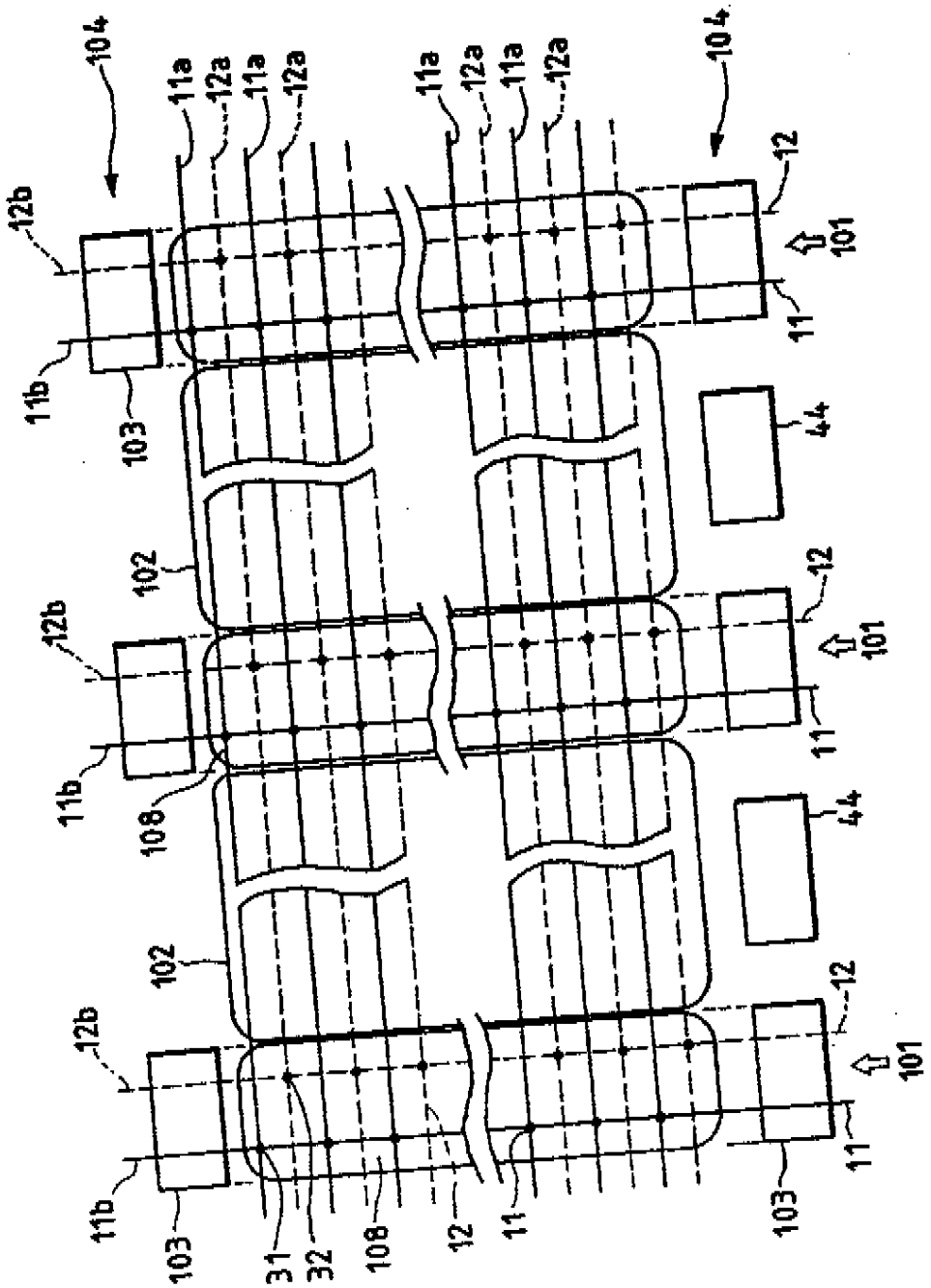

102
100
102
103
102
103
103
102
44
44
104
104
104
104
104
104
104
ROWS 104 OF BACK LAYER CONNECTING REGIONS 44
108
X
101
101
101
101
101
101
101
COLUMNS 101 OF UNIT SENSE AMPLIFIER BLOCKS 108

FIG. 5B


104
11a
12a
11a
12a
11a
12a
11a
12a
104
12b
12
101
11b
11
103
44
102
12b
12
101
11b
11
108
44
102
12b
12
101
11b
11
103
31
32
108
12
11
103

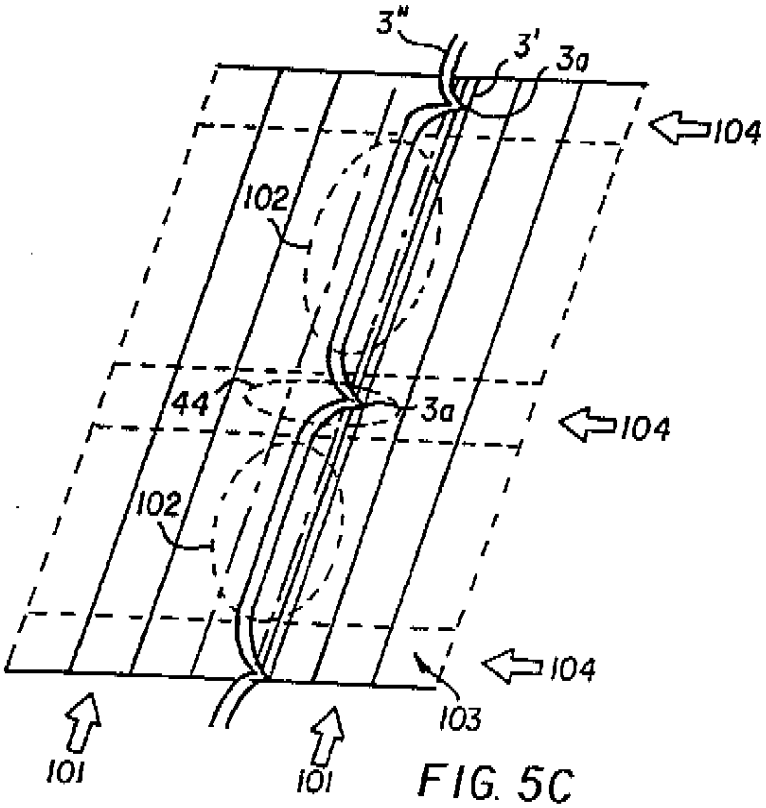

3"
3'
3a
104
102
44
3a
104
102
104
103
101
101

FIG. 5C

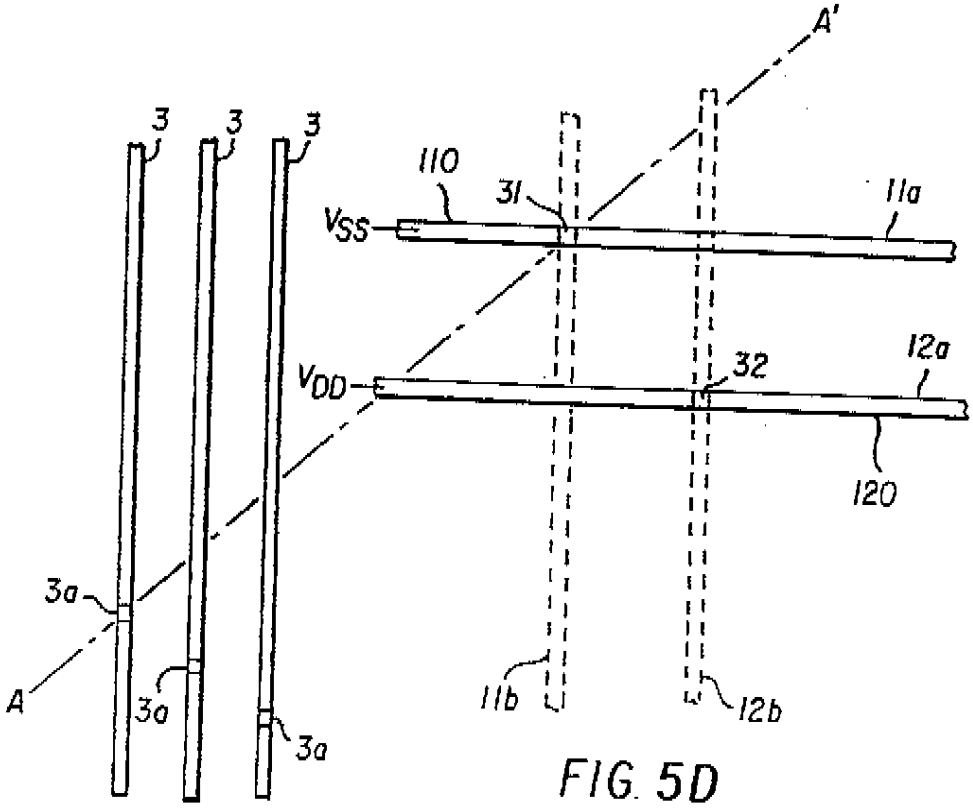

A'
3
3
3
110
31
11a
V_{SS}
12a
32
V_{DD}
120
3a
A
3a
3a
11b
12b

FIG. 5D

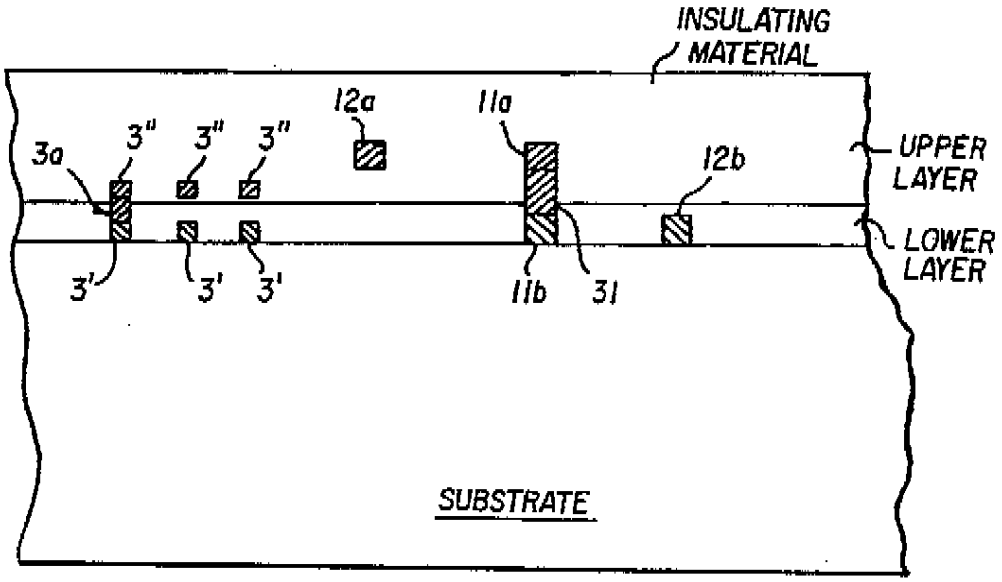

INSULATING MATERIAL
12a
11a
3a
3"
3"
3"
12b
UPPER LAYER
LOWER LAYER
3'
3'
3'
11b
31
SUBSTRATE

FIG. 5E

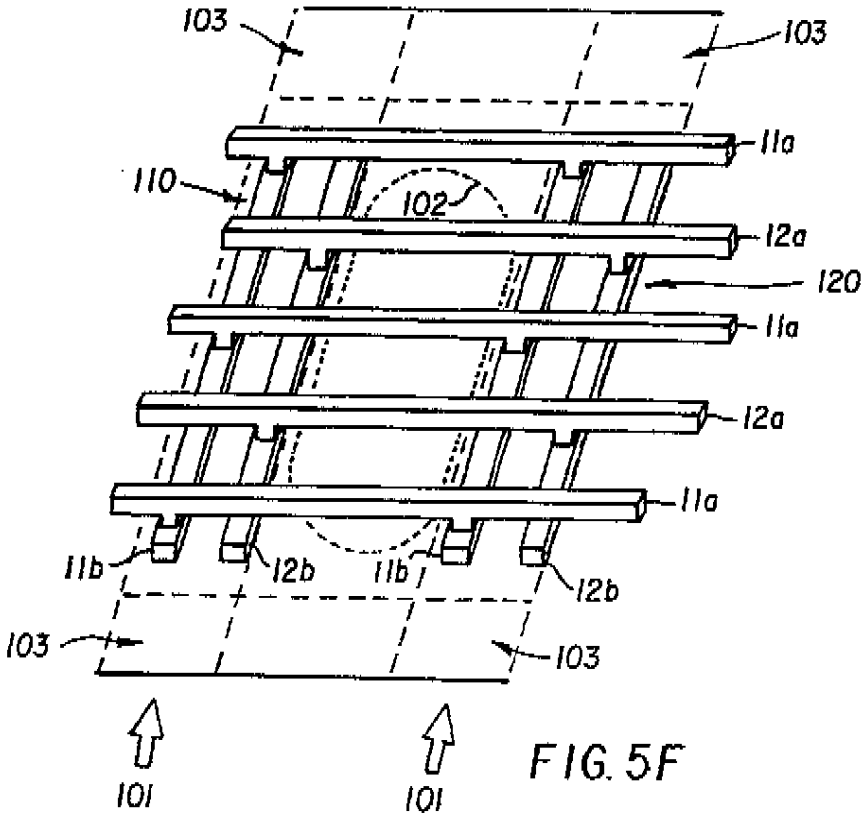
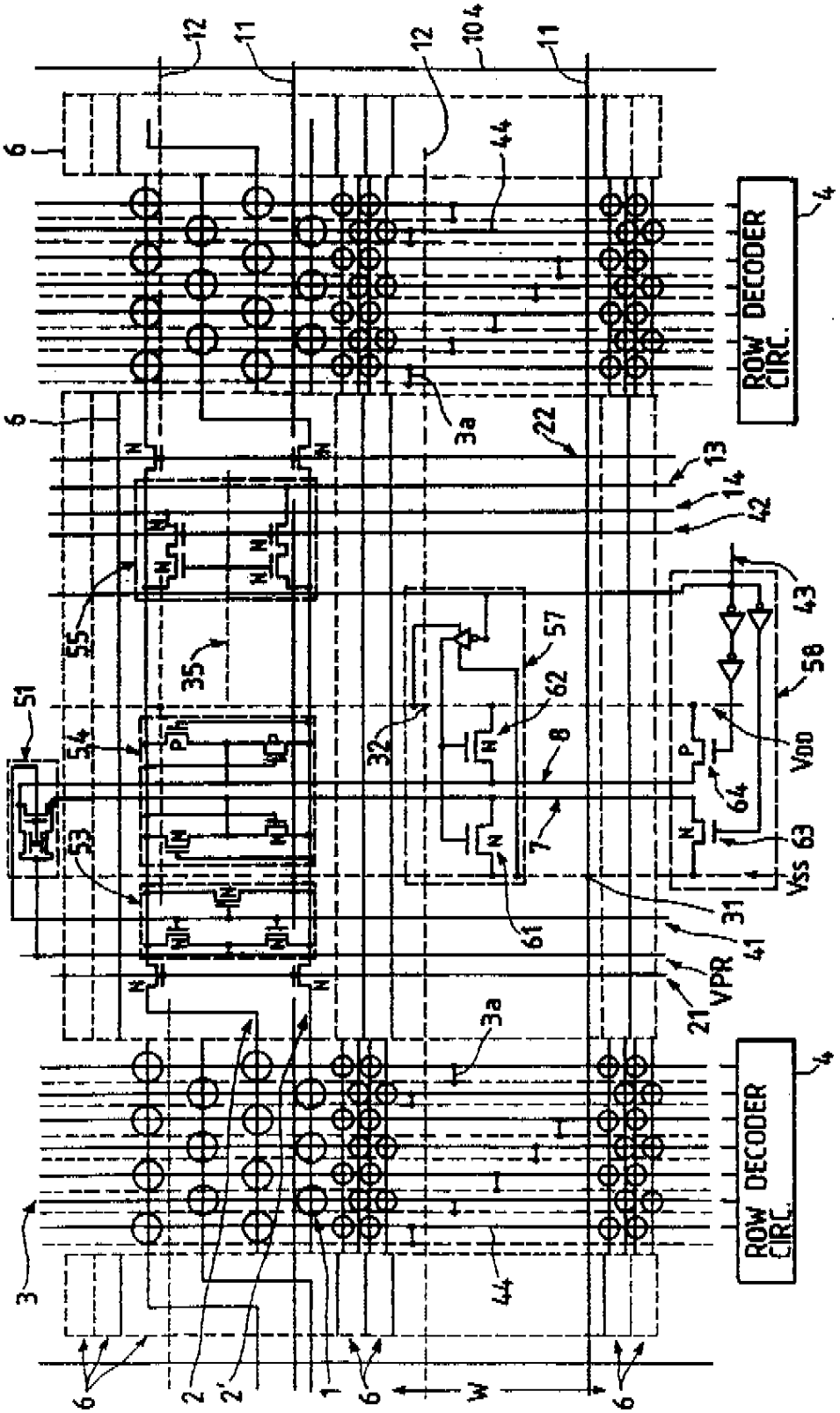

103
103
11a
110
102
12a
120
11a
12a
11a
11b
12b
11b
12b
103
103
101
101

FIG. 5F

FIG. 6A



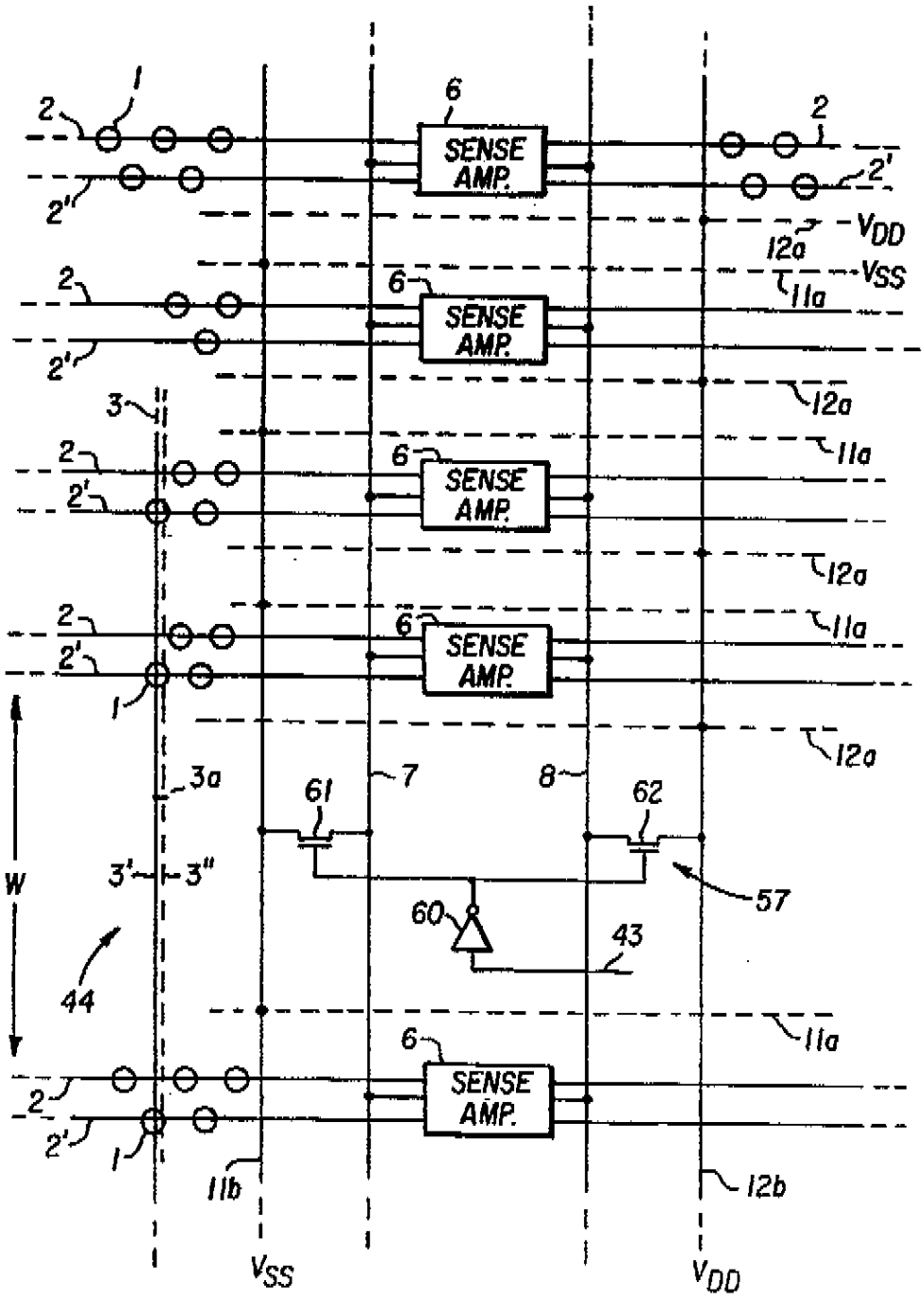
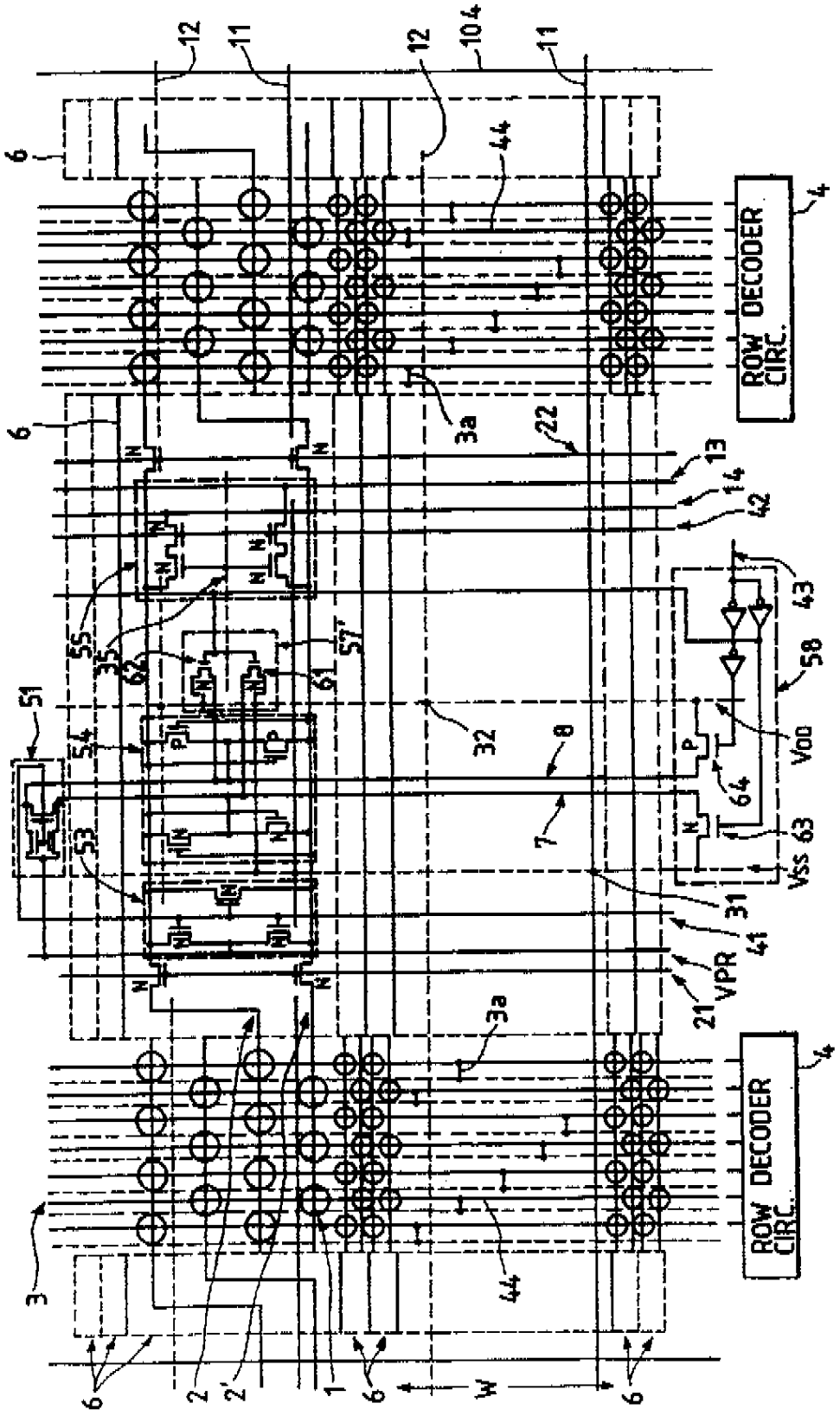

SENSE AMP.
SENSE AMP.
SENSE AMP.
SENSE AMP.
SENSE AMP.
1
2
2'
2''
3
3a
3'
3''
6
61
62
7
8
57
60
43
44
W
11a
11b
12a
12b
V_{DD}
V_{SS}

FIG. 6B

FIG. 7A



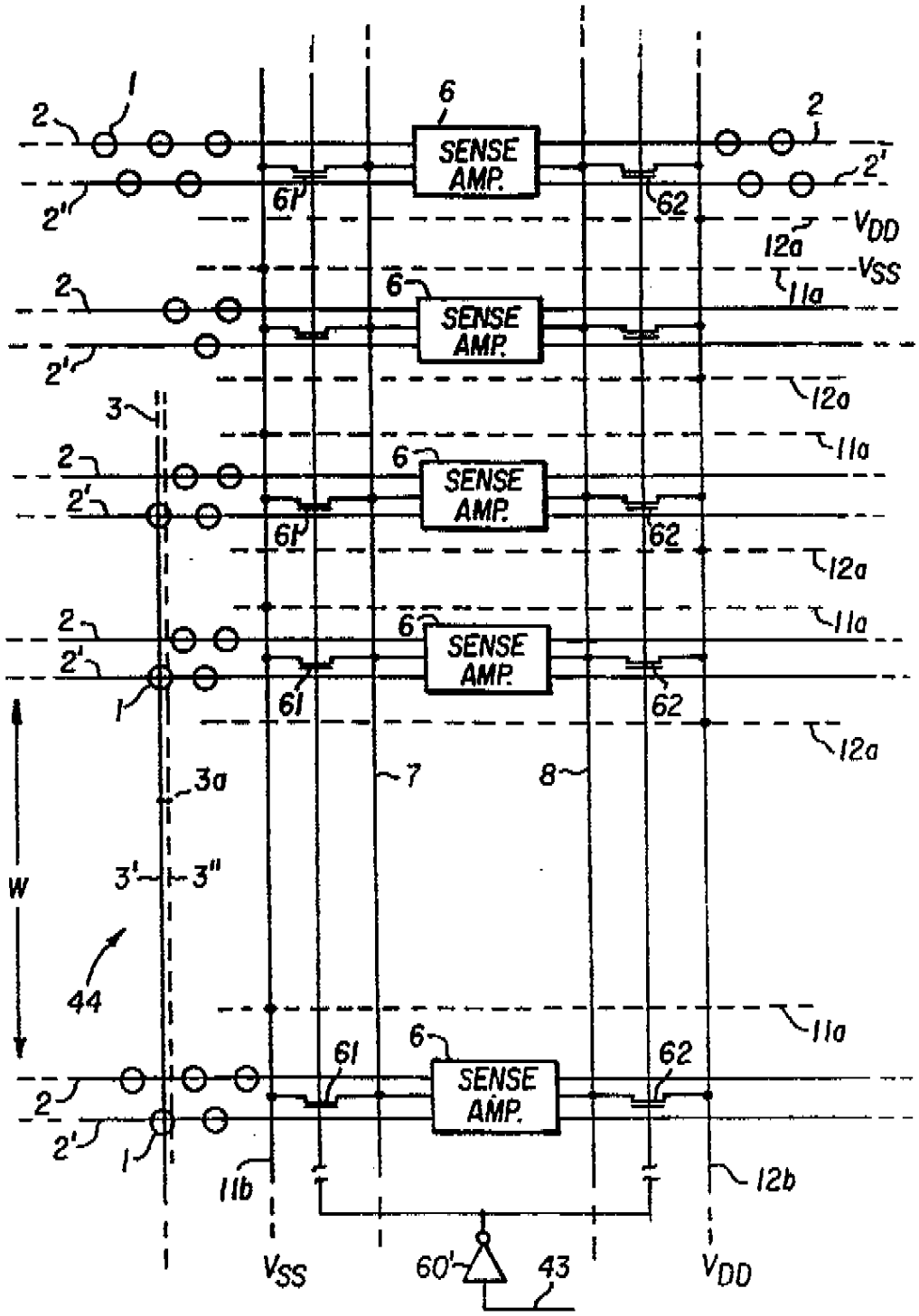

SENSE AMP.
SENSE AMP.
SENSE AMP.
SENSE AMP.
SENSE AMP.
1
2
2'
3
3a
3'
3"
6
61
62
7
8
11a
11b
12a
12b
44
W
V_{DD}
V_{SS}
60'
43

FIG. 7B

FIG. 8

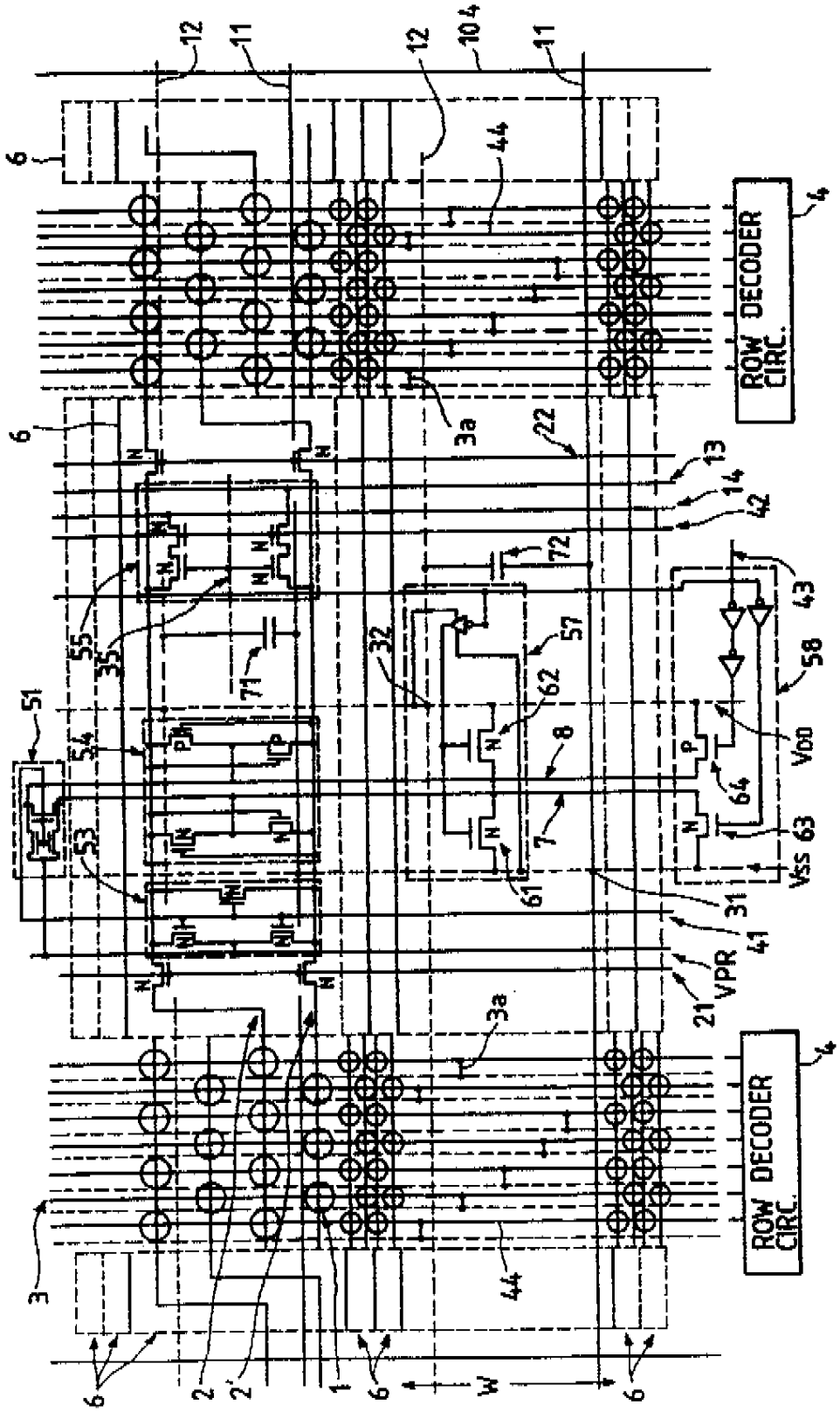


FIG. 9

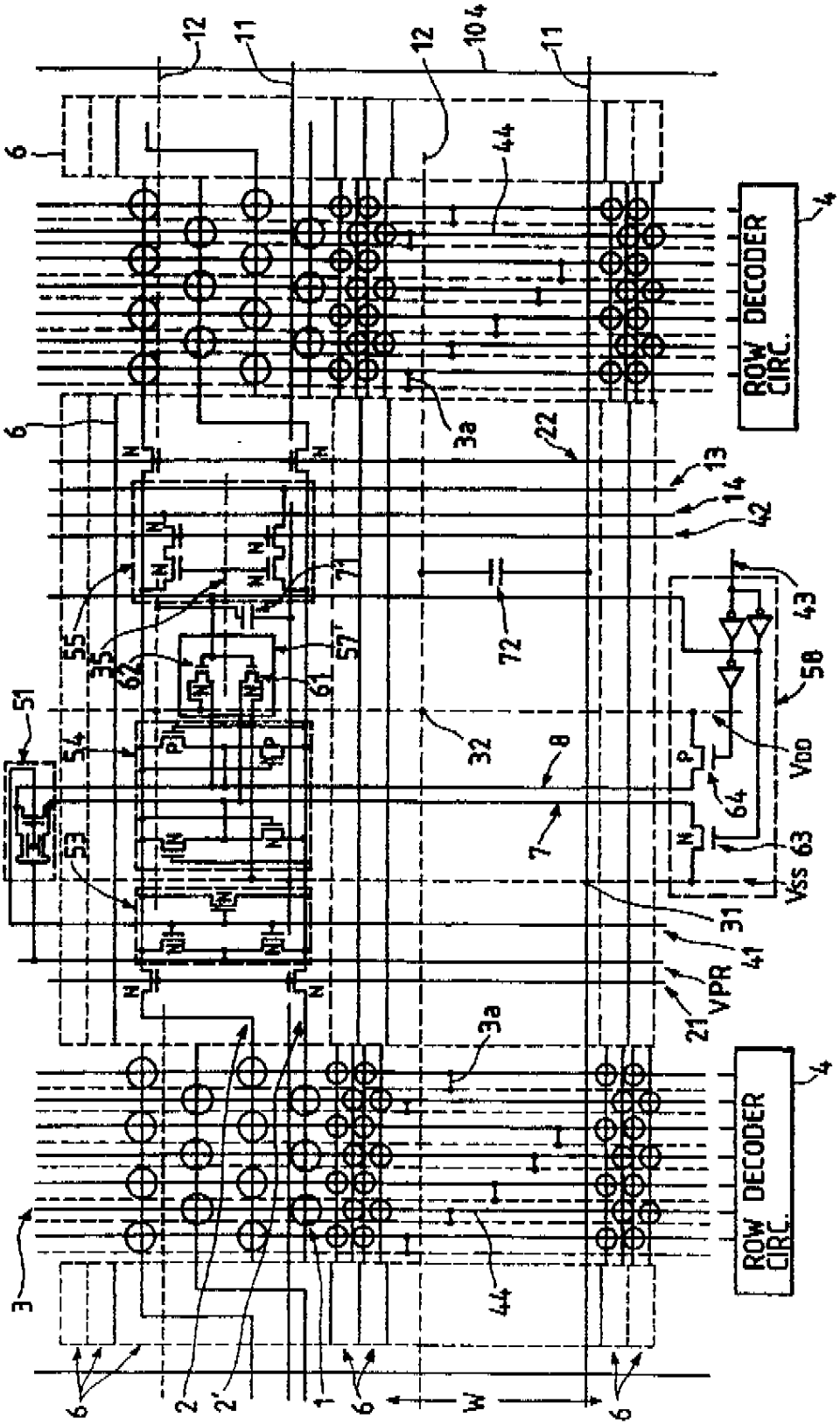


FIG. 10A

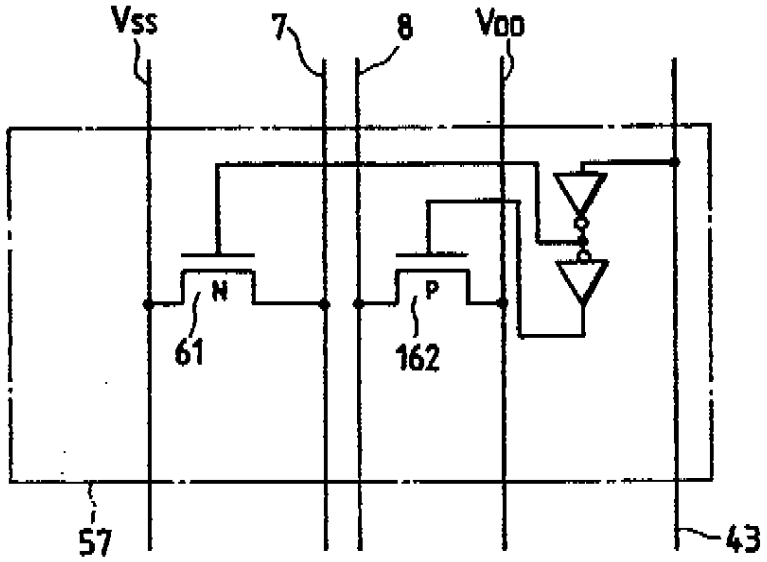
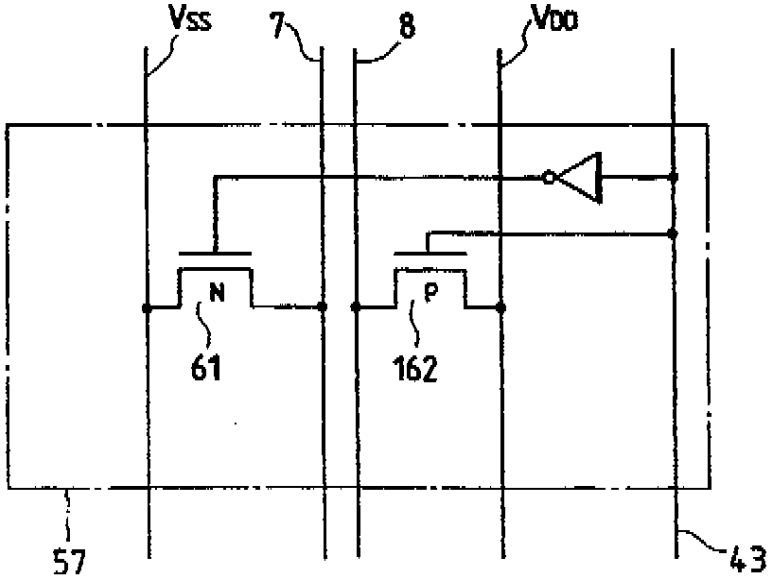


FIG. 10B



SEMICONDUCTOR MEMORY APPARATUS WITH REDUCED LINE WIDTHS

FIELD OF THE INVENTION

The present invention relates to a semiconductor memory apparatus, and in particular to an improved dynamic random access memory (hereinafter referred to as DRAM) integrated circuit wherein the adverse effects of very narrow line widths can be substantially reduced, enabling increased memory capacity or reduced read access times to be achieved.

DESCRIPTION OF THE RELATED ART

In recent years there has been a demand for DRAMs having increased levels of memory capacity and higher access speeds. These are conflicting requirements. To achieve a higher level of memory capacity, i.e. to provide a greater number of memory cells within a specific total area of a DRAM integrated circuit chip, it is necessary to reduce the widths of various connecting lines within the chip. As a result, the line resistance of these is increased, resulting in greater amounts of delay being introduced into the overall memory operation, due primarily to the time required to charge stray capacitances through these high-resistance connecting lines. The main determining factor with regard to the access time of a DRAM (as described in detail hereinafter referring to a specific circuit example) is the time required, following the initiation of a memory read operation for reading out each of respective data values stored in a set of memory cells, before the potential difference between each of the pairs of bit lines of these memory cells is amplified to a specific level by the sense amplifier circuit of the bit line pair. The basic cause of delay in that amplification by the sense amplifier circuits is the time required to charge the bit line pair capacitance, through pairs of sense amplifier drive lines (each coupled in common to a large number of sense amplifier circuits) that are peripherally connected to power supply voltages after a data read operation is initiated. The rate of charging of the bit line pair capacitance of a sense amplifier circuit depends upon the position of the sense amplifier circuit along such a pair of sense amplifier drive lines, i.e. a sense amplifier circuit that is located close to the switches that connect the bit line pair to the power supply voltages will exhibit a relatively low amount of amplification delay, whereas a sense amplifier circuit that is located substantially distant from these switches will exhibit a substantial amount of amplification delay. That delay will be increased in accordance with any reduction of the drive line widths, due to increased line resistance.

Thus, the problem of supplying sufficiently high levels of drive current to all of the sense amplifier circuits of a DRAM during a memory read operation, to ensure a sufficiently low value of read access time, has been the main obstacle in the prior art to achieving even higher degrees of integration, to obtain increased memory capacity.

SUMMARY OF THE INVENTION

It is an objective of the present invention to overcome the disadvantages of the prior art as set out above, by providing a dynamic random access memory formed as an integrated circuit chip, wherein narrower values of connecting line width can be utilized within the chip than have been utilized hitherto, while achieving values of read access time that are similar to or lower than than those of the prior art. The present invention therefore can provide a higher degree of component density, and hence higher memory capacity, without lowering the speed of operation.

These objectives are achieved, basically, by providing a pair of voltage supply meshes, i.e. electrically conducting grids, which extend throughout a region of a DRAM integrated circuit containing memory cells and associated sense amplifiers, with sense amplifier drive circuits being distributed throughout that region, supplied from adjacent points on the nets.

More specifically, the present invention provides a semiconductor memory apparatus including a memory array region having formed therein:

a plurality of unit memory cell blocks distributed through said memory array region at regular spacings, each formed of an array of memory cells;

a plurality of unit sense amplifier blocks distributed among said unit memory cell blocks at regular spacings, each formed of an array of sense amplifier circuits;

a plurality of sense amplifier drive circuits for driving said sense amplifier circuits, distributed among said unit sense amplifier blocks at regular spacings; and

first and second voltage supply meshes, mutually electrically isolated and each extending throughout said memory array region, respectively coupled to receive first and second supply voltages;

each of said sense amplifier drive circuits being coupled to an adjacent point on said first voltage supply mesh to receive said first supply voltage and to an adjacent point on said second voltage supply mesh to receive said second supply voltage.

Each of said said first and second voltage supply meshes is preferably formed of a plurality of first supply lines extending in a first direction and formed in an upper layer of a substrate of said semiconductor memory apparatus and a plurality of second supply lines extending in a second direction and formed in a lower layer of said substrate which is electrically isolated from said upper layer, and a plurality of through-hole connections for interconnecting said first and second supply lines at points of intersection thereof.

Furthermore, each of said first and second supply lines of said first voltage supply mesh is preferably connected to said first supply voltage by at least one end thereof, and each of said first and second supply lines of said second voltage supply mesh is preferably connected to said second supply voltage by at least one end thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a circuit block diagram for describing the basic features of a prior art semiconductor memory apparatus, and FIG. 1B shows the internal configuration of a memory cell for such a semiconductor memory apparatus;

FIG. 2 is a circuit diagram of a sense amplifier circuit of a prior art semiconductor memory apparatus;

FIG. 3 is a waveform diagram for describing the operation of the semiconductor memory apparatus of FIG. 1A;

FIG. 4 is a graph for comparison of a relationship between sense amplifier circuit supply line width and sense amplification delay time, for the prior art example of FIG. 1A and an embodiment of the present invention;

resistance of each of the sense amplifier n-channel FF drive line 7 and sense amplifier p-channel FF drive line 8 is negligible. However in a practical memory circuit, these line resistance values cannot be ignored, and as a result, the voltage waveforms that will actually be developed on the bit lines 2, 2' (in the case of a bit line pair that is located substantially distant from the sense amplifier n-channel FF drive transistor 9 and p-channel FF drive transistor 10) will be of the form shown by the chain-line waveforms B1 and B2 respectively. The reasons for this are as follows. As shown in FIG. 2, the sense amplifier n-channel FF drive line 7 is connected to the point of connection of the source electrodes of the p-channel MOS transistors 17, 18 in a sense amplifier circuit, and in fact is similarly connected in common to each of a large number of sense amplifier circuits. When amplification of the bit line pair potential difference begins during a read cycle, one of the n-channel transistors 17, 18 in FIG. 2 will begin to enter the conducting state, thereby connecting the capacitance of the corresponding one of the bit lines 2, 2' to the sense amplifier n-channel FF drive line 7. Thus although the sense amplifier n-channel FF drive line 7 is now connected at one end to the V_{SS} potential by the sense amplifier n-channel FF drive transistor 9, due to the line resistance of the sense amplifier n-channel FF drive line 7, the potential of that corresponding bit line will begin to fall only gradually towards the V_{SS} potential. A similar effect will occur due to the resistance of the sense amplifier p-channel FF drive line 8, so that the potential of the other one of the pair of bit lines 2, 2' will only gradually begin to rise to the V_{DD} level. Thus the rate of amplification of the potential difference between the bit line pair will bellow, and will be determined by the line resistance values of the sense amplifier n-channel FF drive line 7 and sense amplifier p-channel FF drive line 8, and by the total capacitance of each bit line 2, 2'. The main amplifier 16 is configured such that a data value read out from a memory cell 1 can only be accurately outputted (as a '1' or '0' bit) from the main amplifier 16 when each of the bit line voltage levels has reached a certain threshold value, these being designated as V_H and V_L in FIG. 3. The maximum value of time interval from the start of a read cycle until that condition is reached (i.e. until the actual "worst-case" time point designated as T2 in FIG. 2, rather than the ideal time point designated as T1) is the sense amplification delay time, and determines the read access time of the semiconductor memory apparatus. Thus greatest amount of sense amplification delay time will occur for the sense amplifier circuit that is located farthest from the sense amplifier n-channel FF drive transistor 9 and sense amplifier p-channel FF drive transistor 10, along the sense amplifier n-channel FF drive line 7 and sense amplifier p-channel FF drive line 8 respectively, since in that case there will be maximum values of line resistance through which current must be transferred for driving the bit line potentials to the V_H and V_L levels, so that the bit line waveforms will be of the form of B1 and B2. In the case of a sense amplifier circuit that is located close to the sense amplifier n-channel FF drive transistor 9 and p-channel FF drive transistor 10, since the line resistance values of the sense amplifier n-channel FF drive line 7 and sense amplifier p-channel FF drive line 8 will be relatively small, the bit line waveforms during a read cycle will be close to the ideal waveforms A1 and A2 in FIG. 3.

Since the overall read access time of a semiconductor memory apparatus is determined by the "worst-case" access time, it can be understood that the overall access time will be increased in accordance with any increase in the line resistance of the sense amplifier n-channel FF drive line 7 and sense amplifier p-channel FF drive line 8.

A computer simulation was executed of the read operation of such a prior art DRAM, assuming that to be a 64 Mbit memory, using the SPICE circuit simulator. A relationship was thereby derived between the widths of each sense amplifier n-channel FF drive line 7 and sense amplifier p-channel FF drive line 8 and the sense amplification delay time T_D, designating the width of each sense amplifier n-channel FF drive line 7 as W_{AL} and assuming that the width of each sense amplifier p-channel FF drive line 8 is equal to $W_{AL} \times 0.2$, and also assuming that these lines are formed of aluminum with a thickness of 0.8 μm. The result is plotted as the curve Z1 in FIG. 4. As can be seen from that curve Z1, as the width value W_{AL} is reduced, the sense amplification delay time T_D suddenly begins to increase sharply, after a delay time of approximately 8 ns has been exceeded. It can thus be understood that with such a prior art DRAM, not only is the sense amplification delay time inherently excessively long, but also, if the widths of the supply lines 7 and 8 are made smaller, in order to achieve a higher degree of integration of the DRAM for thereby obtaining increased memory capacity, then the value of the sense amplification delay time will rapidly become extremely high. Thus this has presented a considerable obstacle to achieving both an increased degree of component density and a higher speed of operation for a DRAM, in the prior art.

FIG. 5A is a diagram for describing the basic configuration of a first embodiment of a semiconductor memory apparatus according to the present invention, while FIG. 5B shows details of the interior of an outlined region designated as X in FIG. 5A. In the prior art example of FIG. 1A described hereinabove, each of the word lines 3 is shown as a single conductor. However it is now usual practice in the art to configure each of the word lines 3 as a pair of connecting lines that are disposed mutually adjacent in parallel and separated by a layer of electrically insulating material, for example a lower line formed of polysilicon, in a lower circuit layer in which are formed the transistors and capacitors etc. of the memory, and an upper line, formed of aluminum, which is disposed in a "back layer" above that lower circuit layer. Such an arrangement can provide lower values of line resistance for the word lines, enabling more rapid rise and fall times of potential on the word lines. However to achieve that lowered resistance it is necessary to interconnect each upper line to its corresponding lower line, by through-hole connections, at periodic spacings from the top to bottom of the word line. It is therefore necessary to provide regions in which such through-hole connections are formed, which are outside the regions in which memory cells are formed. Such regions will be referred to in the following as back layer connecting regions. In FIG. 5a, 100 denotes a memory array region in which are formed arrays of memory cells and sense amplifier circuits, in a DRAM integrated circuit chip. Numerals 102 denote respective unit memory cell blocks, each consisting of an array of a fixed number of memory cells. As shown, these unit memory cell blocks 102 are formed as successive columns, each column containing a plurality of unit

FIGS. 5A-5B are diagrams for illustrating the basic configuration of a first embodiment of a semiconductor memory apparatus according to the present invention;

FIGS. 6A-6B is a diagram showing details of a portion of the circuit of the first embodiment;

FIGS. 7A-7B, 8 and 9 are partial circuit diagrams showing details of second, third and fourth embodiments of the present invention, respectively; and

FIGS. 10A and 10B show alternative circuit configurations for a sense amplifier drive circuit 57 in the embodiments of FIGS. 6 and 9 respectively.

DESCRIPTION OF PREFERRED EMBODIMENTS

For a better understanding of the preferred embodiments, an example of a prior art semiconductor memory apparatus will first be described, for comparison of the prior art with the semiconductor memory apparatus of the present invention.

FIG. 1A is a simplified circuit diagram for describing the basic configuration of a prior art DRAM, which will be assumed to be formed as an integrated circuit based on n-channel and p-channel MOS transistors (metal-oxide silicon field-effect transistors) used as switching-elements and amplifier elements. In FIG. 1A the numerals 1 denote respective memory cells, each for storing one data bit, and 2 and 2' denote a pair of bit lines each coupled to a row of the memory cells 1, for transferring output signals produced from memory cells 1 (i.e. outputted from a memory cell in accordance with an amount and polarity of electrical charge that has been previously stored in the cell to represent a data bit). Numerals 3 denote respective word lines, each coupled to a column of the memory cells 1, for selecting specific ones of the memory cells 1 for read/write operations, and 4 denotes a row decoder circuit for producing row selection signals to select a specific one of the word lines 3. The numerals 6 denote respective sense amplifier circuits, each of which is coupled to receive output signals transferred from memory cells 1 via a corresponding pair of bit lines 2, 2', for amplifying minute amounts of potential difference that are thereby produced between such a corresponding bit line pair when a memory cell is read. Numeral 5 denotes a column decoder circuit, for selecting an amplified output data signal of one of the sense amplifier circuits 6. As described hereinafter, each of the sense amplifier circuits 6 in such a DRAM is based upon an n-channel flip-flop (i.e. a flip-flop circuit formed of n-channel MOS transistors) and a p-channel flip-flop, with these flip-flops being connected between the corresponding bit line pair 2, 2' during a memory read operation, and with the flip-flops being respectively triggered in accordance with the polarity of the minute potential difference that is developed between that bit line pair during a memory read operation, to thereby amplify that potential difference. Numeral 7 denotes a sense amplifier n-channel flip-flop drive line, which is connected in common to the n-channel flip-flops of each of the sense amplifier circuits 6, for driving the source electrodes of these flip-flops (from an initial precharge potential, described hereinafter) towards the V_{SS} power supply potential during a memory read operation. In the this embodiment, the V_{SS} power supply potential is at ground potential. Numeral 9 denotes an MOS transistor which functions as a sense amplifier n-channel flip-flop (FF) drive switching transistor, which is controlled to connect the lower end of the sense amplifier n-channel FF drive line 7 to the V_{SS} potential during a memory read operation. Numeral 8 denotes a sense amplifier p-channel FF drive line, which is connected in common to the p-channel flip-flops of each of the sense amplifier circuits 6, for driving the source electrodes of these flip-flops towards the V_{DD} power supply potential during a memory read operation. Numeral 10 denotes an MOS transistor which functions as a sense amplifier p-channel FF drive switching transistor, which is controlled to connect the lower end of the sense amplifier p-channel FF drive line 8 to the V_{DD} potential during a memory read operation. Numeral 11 denotes a ground line, for connecting the sense amplifier n-channel FF drive transistor 9 to the Vss potential, and 12 denotes a power supply line for connecting the the sense amplifier p-channel FF drive transistor 10 to the V_{DD} power supply potential. 13 and 14 denote data lines, for outputting data produced from the sense amplifier circuits 6. Numeral 16 denotes a main amplifier, coupled to receive data which are transferred via the data lines 13 and 14.

FIG. 1B shows a specific circuit configuration for each of the memory cells 1, in which 1*a* denotes a capacitor for storing electrical charge representing a data bit, and 1*b* denotes a MOS transistor which is controlled by the selection signal applied to the corresponding word line 3, for transferring charge between the capacitor 1*a* and the corresponding bit line 2, for reading and writing data to/from the memory cell.

FIG. 2 shows an example of a circuit for each sense amplifier circuit 6. In FIG. 2, numerals 17, 18 denote n-channel MOS transistors, 19, 20 denote p-channel MOS transistors, which are interconnected to form the aforementioned n-channel and p-channel FFs of the sense amplifier circuit, while 15*a* and 15*b* denote respective MOS transistors serving as switches for selectively connecting the bit line pair 2, 2' to the data lines 13 and 14.

The operation of this prior art sense amplifier circuit in a memory read sequence is as follows, considering only one of the bit line pairs. Firstly, one of the word lines 3 is selected by the row decoder circuit 4. As a result, data (as electrical charge) from the memory cell 1 which is connected to that word line 3 will be outputted, e.g. to the bit line 2. A minute potential difference will thereby be generated between the bit lines 2, 2', which will be amplified by the sense amplifier circuit 6. The amplified data value is transferred through the switch transistors 15*a*, 15*b* and the data lines 13, 14, to be amplified by the main amplifier 16, then outputted from the memory chip. The operating waveforms areas shown in FIG. 3, in which a time interval A denotes a precharge interval, in which the bit lines 2, 2' are charged to a fixed potential. During the succeeding time interval B, the selected word line 3 is driven, so that the charge stored in a memory cell 1 is transferred as a signal to the bit line 2, i.e. is read out as a minute potential difference appearing between the bit lines 2, 2'. In the succeeding time interval C, the sense amplifier circuit 6 amplifies that potential difference, then the data that was read out from the memory cell 1 is rewritten back into the cell. In the succeeding time interval D, in preparation for the next read cycle, all of the bit lines 2, 2' are again charged to the fixed precharge potential, i.e. this is again a precharge interval.

In FIG. 3, the full-line portions A1, A2 denote the voltage waveforms that would appear on the bit lines 2, 2' respectively, in an ideal condition in which the line

memory cell blocks disposed at regular spacings. Numerals **108** denote respective unit sense amplifier blocks, each formed of a plurality of sense amplifier circuits and disposed between two adjacent unit memory cell blocks **102**, along the horizontal direction of the drawings. Numerals **104** denote horizontally elongated regions each containing a row of back layer connecting regions **44**, formed between vertically adjacent unit memory cell blocks **102**. Numerals **101** denote respective columns of blocks of sense amplifier circuits. Numerals **103** denote respective regions of intersection between the columns of sense amplifier blocks **101** and the row region **104** of back layer connecting regions **44**. Respective sense amplifier drive circuits are formed in these regions **103**, i.e. with each region **103** being disposed between two adjacent back layer connecting regions.

It can thus be understood from FIGS. 5A and 5B that with the present invention, sense amplifier drive circuits are distributed throughout the memory array region, rather than being disposed only at the periphery of that region as in the prior art. It can further be understood that in this embodiment of the invention, each of the unit memory cell blocks **102** has one of these sense amplifier drive circuits respectively disposed at each of the four corners of that unit memory cell block. Typically, each unit sense amplifier block will contain a total of 64 sense amplifier circuits.

FIG. 5C is a simple conceptual oblique view to illustrate how each word line **3** consists of an upper line **3''** which is formed of metal, and a lower line **3'** which is formed of polysilicon, and how these two lines **3'', 3'** are periodically interconnected by through-hole connections **3***a* within the back layer connecting regions **44**.

In FIG. 5B, the designations **11***a* indicated respective ones of a plurality of power supply lines extending in a first direction which is shown in the drawing as the vertical direction, while the designations **11***b* indicate respective ones of a corresponding plurality of power supply lines each extending in a second direction that is shown in the drawing as the horizontal direction. The lines **11***a* and **11***b* are mutually insulated by being formed in respectively different layers. The lines **11***a* may for example be formed in an uppermost layer of the integrated circuit chip, while the lines **11***b* are formed in a layer that is disposed below that uppermost layer and electrically isolated from that uppermost layer and which also contains the transistor elements.

The sets of lines **11***a*, **11***b* are mutually electrically connected at their points of intersection by respective through-hole connections **31**, to form an electrically conducting mesh **110** (which in this embodiment is in the shape of a rectangular grid). At least one end of each of the power supply lines **11***a* and **11***b* is connected to the V_{SS} power supply voltage, which in this embodiment is at ground potential. The mesh **110** will be referred to in the following as the V_{SS} supply mesh. The designations **12***a* indicate respective ones of a plurality of power supply lines each extending in the first direction, i.e. the vertical direction as viewed in FIG. 5B, which may be formed in the same upper layer of the integrated circuit chip as the lines **11***a*, while the designations **12***b* indicate respective ones of a corresponding plurality of horizontally extending power supply lines which are formed in the aforementioned lower layer, and so are electrically isolated from the lines **12***a*. The sets of lines **12***a*, **12***b* are mutually electrically connected at their points of intersection by respective through-hole connections **32**, to form a second electrically conducting mesh **120**. At least one end of each of the power supply lines **12***a*, **12***b* is connected to the V_{DD} power Supply voltage, and the mesh **120** will be referred to in the following as the V_{DD} supply mesh.

FIG. 5F is a conceptual oblique view to illustrate part of the power supply meshes **110**, **120** as described hereinabove. For ease of understanding, the thickness of each line of the meshes has been greatly enlarged.

It can be understood that with this embodiment, the Vss supply mesh **110** and Vdd supply mesh **120** are dispersed throughout the regions **101** which contain columns of sense amplifier circuits, and also throughout the regions **104** in which are formed the back layer connecting regions and in which (in this embodiment) are also formed the sense amplifier drive circuits, in the intersection regions **103**. Thus both the Vss supply mesh **110**, Vdd supply mesh **120** and the sense amplifier drive circuits are dispersed throughout the memory area, so that each of the sense amplifier drive circuits (which are dispersed throughout the memory array region rather than located only at the periphery, as mentioned above) can be connected to the nearest points thereto on the Vss supply mesh **110** and Vdd supply mesh **120** to receive the V_{SS} and V_{DD} supply voltages respectively. Thus the lengths of the paths between each sense amplifier drive circuit and the Vss supply mesh **110** and Vdd supply mesh **120** can be minimized. Moreover the distances between the sense amplifier circuits and the sense amplifier drive circuits can also be made much shorter than has been possible in the prior art, thereby providing various advantages over a prior art type of DRAM, as described in detail hereinafter. In addition, each sense amplifier drive circuit drives a smaller number of sense amplifier circuits than is possible in a prior art semiconductor memory apparatus, in which sense amplifier drive circuits are not distributed throughout the memory cell array.

FIG. 5D is a simplified partial plan view to illustrate part of the word lines **3** and the power supply meshes **110**, **121** of this embodiment. For ease of understanding, the spacings shown between the work lines and supply mesh conductors have been altered from those of a practical apparatus. The through-hole interconnections between the upper and lower lines **3'', 3'** of each word line **3** are each designated as **3***a*, while the through-hole interconnections between the lines **11***a*, **11***b* of the supply mesh **110** and between the lines **12***a*, **12***b* of the supply mesh **120** are respectively designated as **32** and **32**.

FIG. 5E is a cross-sectional view in elevation corresponding to FIG. 5D, taken along the line A—A' of FIG. 5D. As illustrated, the lower lines **3'**, **11***b* and **12***b* are each formed of suitably doped polysilicon, within a polysilicon layer formed on a substrate. Various other circuit elements such as transistors are also formed in that polysilicon layer. As shown, the upper lines **3''** and **11***a*, **12***a* of the word lines and supply meshes are formed as respective metal lines in an upper layer, above and insulated from the polysilicon lower layer in which the lower lines are formed.

FIGS. 6A and 6B are respective partial circuit diagrams of the first embodiment. FIG. 6A shows the basic configuration whereby a sense amplifier drive circuit **57** (formed of FETs **61**, **62** and inverter **60**) is positioned within two vertically adjacent unit sense amplifier blocks. In FIG. 6A, the conductors **11***a*, **11***b*, **11***a*, **12***b* of the supply meshes, and lines which can be coupled to

the supply meshes, are shown in heavy black lines, to distinguish these from normal signal lines. FIG. 6B shows more details of the circuit, including internal configuration of a sense amplifier circuit 6.

To avoid excessive complexity in the drawing, some of the connecting lines have been omitted or are shown only partially, while some of the dimensional relationships have been distorted for ease of understanding. The configuration of a region 104 will first be described in which a row of back layer connecting regions are formed and in which, in this embodiment, sense amplifier drive circuits are also formed. In FIG. 6A, 6B the reference numerals 6 designate respective sense amplifier circuits, each of which can be connected to a pair of bit lines 2, 2' coupled to memory cells 1 in a memory cell region to the right or to the left of that sense amplifier circuit. As shown, the sense amplifier circuits 6 are arranged in unit blocks within successive vertically extending columns, with these unit blocks positioned in correspondence with memory cell regions to either side, and with each unit block consisting for example of a total of 64 sense amplifier circuits. In FIG. 6B, one of the sense amplifier circuits 6 is shown in detail, expanded in size, while the contents of one of the regions 104 are also shown in detail, expanded in size to show a sense amplifier drive circuit 57 and the width W (indicated by arrows) of each region 44,

FIG. 6B also shows row drive circuits 4, each of which drives a column of unit memory cell blocks shown, and a sense amplifier drive circuit 58 which serves to ensure satisfactory rewriting of memory cell contents after each read operation, as described in detail hereinafter, and which operates in conjunction with a column of dispersed sense amplifier drive circuits 57. Numeral 41 denotes a precharge control line, 42 denotes a sense amplifier column selector line and 43 a sense amplifier activation line. In addition, 51 denotes a sense amplifier control line precharge circuit, 53 denotes a precharge control circuit, 54 denotes a sense amplifier flip-flop circuit, formed of an n-channel FF and a p-channel FF as shown, and 55 denotes a data transfer circuit.

In the embodiment of FIG. 6, each of the regions 103 shown in FIGS. 5A, 5B has one of the sense amplifier drive circuit 57 formed therein. In a sense amplifier drive circuit 57, 61 and 62 denote n-channel MOS transistors for sense amplifier driving, which are connected to the sense amplifier n-channel FF drive line 7 and sense amplifier p-channel FF drive line 8 respectively. In the sense amplifier drive circuit 58, 63 denotes an n-channel MOS transistor for sense amplifier driving, which is connected to the sense amplifier n-channel FF drive line 7, while 64 denotes a p-channel MOS transistor for sense amplifier driving which is connected to the sense amplifier p-channel FF drive line 8.

Each of the word lines 3 is formed of an upper and a lower conductor, formed in an upper and a lower layer which are mutually electrically isolated. Each upper conductor of a word line 3 is connected to the corresponding lower conductor by means of a through-hole connection 3a, as indicated in FIG. 6. Sets of these through-hole connections 3a are formed in respective ones of the aforementioned regions 44, between the memory cell regions that are successively arranged in a vertical column, with each set of word lines 3 of such a column being driven by a corresponding row decoder circuit 4.

In the following, for brevity of description, the combination of the aforementioned bit line precharge circuit 53, CMOS FF amplifier circuit 54 and data transfer circuit 55, in conjunction with a pair of n-channel MOS transistors that are controlled by the shared switch gate control line 21 and a pair of n-channel MOS transistors that are controlled by the shared switch gate control line 22, will be referred to as a sense amplifier circuit, although actual amplification is executed by the CMOS FF amplifier circuit 54. A column of such sense amplifier circuits 6 is disposed between each pair of adjacent columns of memory cell regions, and sense amplifier drive circuits 57 are distributed throughout each column of sense amplifier circuits 6, i.e. with one sense amplifier drive circuit 57 being disposed in each of the regions 103 between two horizontally adjacent back layer connecting regions 44, as described above. Each sense amplifier drive circuit 57 is connected to the Vss supply mesh 110 and the Vdd supply mesh 120 at respective nearest points on these meshes to that circuit 57. Thus as can be understood from FIG. 6, the length of each connecting line between a sense amplifier drive circuit 57 and a power supply mesh can be made extremely short.

The operation of this embodiment will first be described for the case of data read-out from a memory cell 1. For simplicity, the description will be given with reference to the sense amplifier circuit 6 whose internal circuit is shown in detail in FIG. 6B, and the bit line pairs 2, 2' that are coupled to that sense amplifier circuit. Firstly, when the charge stored as a data value in a memory cell 1 is to be read out, the bit lines 2, 2' are each set to the precharge potential Vpr. The shared switch gate control lines 21 and 22 are each set to high level potential, so that each of the sense amplifier circuits 6 becomes connected to the memory cell regions that are positioned at the left and at the right of it. Next, the precharge control line 41 is set to the high level potential, so that the bit line precharge circuit 53 charges the bit lines 2, 2' both within the sense amplifier circuit 6 and within the memory cell regions that are located to the left and right of that sense amplifier circuit 6, to the precharge voltage Vpr. At the same time the sense amplifier control line precharge circuit 51, which is located at the upper end of the column of sense amplifier circuits 6, simultaneously charges the sense amplifier n-channel FF drive line 7 and sense amplifier p-channel FF drive line 8 to the precharge voltage Vpr. Next, the shared switch gate control line for the memory cell region that is not to be read out, for example the line 22 which controls read-out of data from the memory cells to the right of the sense amplifier circuit 6, is set to the low level potential, so that only the unit memory cell block from which read-out is to be effected remains connected to the sense amplifier circuit 6. One of the word lines 3 is then selected by the row decoder circuit 4, whereby that word line rises to the high level potential. As a result, the charge that is held in a corresponding one of the memory cells that is coupled to the bit line pair 2, 2' is transferred to one of these bit lines, causing a minute potential difference to be produced between these bit lines 2, 2'. That potential difference is then amplified by the sense amplifier circuit 6. That amplification begins after the sense amplifier activation line 43 is set to the low level potential, whereby each of the n-channel MOS transistors 61, 62 in the sense amplifier drive circuit 57 (and in all of the other sense amplifier drive circuits of that column of sense amplifier

circuits, each sense amplifier drive circuit 57 being located between two horizontally adjacent ones of the back layer connecting regions 44 as described hereinabove) is set in the conducting state, so that the potential of the sense amplifier n-channel FF drive line 7 approaches the ground potential (V_{SS}), while the potential of the sense amplifier p-channel FF drive line 8 approaches the power supply potential V_{DD}. Latching operation of the flip-flops that are formed within the CMOS FF amplifier circuit 54 thereby occurs, providing amplification of the minute potential difference between the bit line pair 2, 2'.

The sense amplifier column selector line 42 is then set to the high level potential, and the column selector line 35 is then also set to the high level potential, whereby the signal state within the sense amplifier circuit 6 that results from the triggering of the flip-flops is transferred, via the data transfer circuit 55, to be outputted via the data lines 13 and 14. That signal is thereafter further amplified, and then outputted from the memory chip.

In parallel with the data read-out operation described above, an operation is effected for rewriting the read-out data back into the memory cell from which it was-read. This is executed by the sense amplifier drive circuit 58, which is disposed at the lower end of the column of sense amplifier circuits 6. When the sense amplifier activation line 43 is set to the low level potential, the n-channel MOS transistors 63, 64 within the sense amplifier drive circuit 58 are each set in the conducting state, whereby the sense amplifier n-channel FF drive line 7 is caused to approach the potential V_{SS} even more closely than it is brought by the action of the various sense amplifier drive circuits 57 in that column of sense amplifier circuits 6, and the sense amplifier p-channel FF drive line 8 is similarly brought even closer to the V_{DD} supply potential.

The above operations complete the read operation sequence executed by the sense amplifier circuit 6, with the data read out from the memory cell 1 having been outputted from the memory chip.

In the above embodiment, an n-channel MOS transistor 62 is used in each sense amplifier drive circuit 57 for driving the p-channel FFs of the sense amplifier circuits via the sense amplifier p-channel FF drive line 8. As a result, the potential of the sense amplifier p-channel FF drive line 8 will not rise completely to the V_{DD} supply voltage during a read operation, but will differ from V_{DD} by an amount that is equal to the threshold voltage of the MOS transistor 62. Thus, data rewriting back into a memory cell after a read operation cannot be effected in a completely satisfactory manner by the operation of these sense amplifier drive circuits 57 alone. However the reasons for using an n-channel MOS transistor in each sense amplifier drive circuit 57 are as follows. If a p-channel MOS transistor were to be used in place of the n-channel transistor 62 in each sense amplifier drive circuit 57, then it would also be necessary to use an additional pair of inverters within the sense amplifier drive circuit 57, if the sense amplifier column selector line 42 is directly connected to each sense amplifier drive circuit 57 as in FIG. 6. This would result in additional space being required in the width of each row 104 of back layer connecting regions 44, making the design rules even stricter. That problem could be overcome by connecting the sense amplifier activation line 43 through a single inverter (e.g. one of the inverters in the sense amplifier drive circuit 58) to all of the sense amplifier drive circuits 57, however in that case it would be necessary to use an inverter having a sufficiently high degree of current drive capacity for that purpose. Moreover it is advantageous to use an n-channel MOS transistor as the transistor 62 in each sense amplifier drive circuit 57, since in general, for a specific size of transistor (i.e. size of substrate area occupied), an n-channel MOS transistor has a greater current drive capability than a p-channel MOS transistor. Thus, savings in space are achieved by using n-channel MOS transistors.

Thus as described above, each sense amplifier drive circuit 57 functions primarily during the stage of data read-out, with the level of voltage to which the sense amplifier p-channel FF drive line 8 is driven during that stage by the sense amplifier drive circuits 57 being sufficiently high to ensure satisfactory amplification operation by the sense amplifier circuits 6. The purpose of the sense amplifier drive circuit 58, as mentioned hereinabove, is to ensure that the sense amplifier p-channel FF drive line 8 as well as the sense amplifier n-channel FF drive line 7 will then be driven to values that are sufficiently close to the V_{DD} and V_{SS} values respectively to ensure satisfactory rewriting of data back into the memory cells. For that reason, a p-channel MOS transistor is used in the sense amplifier drive circuit 58 for driving the sense amplifier p-channel FF drive lines, so that the problem that is encountered when an n-channel MOS transistor is used for such a drive function (i.e. caused by the transistor threshold voltage) does not arise.

The following results are achieved from a DRAM memory having the configuration described above. Firstly, the problem of sense amplification delay, resulting from the resistance values of the drive lines 7 and 8 as described hereinabove, can be substantially completely overcome. This is due to the fact that a plurality of sense amplifier drive circuits 57, for driving the sense amplifier circuits 6 during data read-out, are distributed throughout each column of sense amplifier circuits 6, along the sense amplifier circuit drive lines 7 and 8, so that the average distance between each sense amplifier circuit 6 and a sense amplifier drive circuit 57 (i.e. as measured along the direction of the sense amplifier drive lines 7 and 8) can be made from $\frac{1}{8}$ to 1/32 times the distance in the case of a prior art DRAM. The amounts of effective line resistance of the drive lines 7 and 8 are thereby correspondingly reduced, and hence the desired reduction of the sense amplification delay time can be achieved. The present invention is the first DRAM memory apparatus to make such a result possible, which is made feasible by the provision of the Vss supply mesh 110 and Vdd supply mesh 120, since these enable the aforementioned distribution of the plurality of sense amplifier drive circuits 57 throughout each column of sense amplifier circuits 6, and ensure that each sense amplifier drive circuit 57 can provide a sufficiently high level of drive current.

As was done for the prior art example described hereinabove, the operation of a 64 Mbit DRAM in accordance with the above embodiment was simulated, using the SPICE circuit simulator. The relationship between the widths of the sense amplifier n-channel FF drive line 7 and sense amplifier p-channel FF drive line 8 and the sense amplification delay time T_D was thereby obtained, designating the width of each sense amplifier n-channel FF drive line 7 as W_{AL} and assuming that the width of each sense amplifier p-channel FF drive line 8 is equal to $W_{AL} \times 0.2$, and also assuming that these lines

are formed of aluminum with a thickness of 0.8 m, as for the prior art example. The result is plotted as the curve Z2 in FIG. 4. As will be clear from that curve, the sense amplification delay time T_D is approximately 4 ns, so that the delay time is reduced by at least 4 ns by comparison with the prior art example. Moreover, as the widths of the supply lines 7 and 8 are reduced, and even if these are made extremely narrow, there is almost no change in the sense amplification delay time. Thus by comparison with the prior art, the first embodiment of the present invention enables the sample delay time to be made extremely small, while in addition the widths of the supply lines 7 and 8 for driving the n-channel FFs and p-channel flip-flops respectively of the sense amplifier circuits can be made narrower than has been possible in the prior art, thereby enabling a higher degree of integration to be achieved than has been possible in the prior art, without the danger of an increase being produced in the sense amplification delay time T_D. The first embodiment therefore enables the objectives of both increased speed of operation and increased circuit scale, i.e. increased memory capacity, to be both realized.

A second embodiment of the present invention will be described referring to FIGS. 7A and 7B. This embodiment differs from the first embodiment of FIG. 6 only in that the sense amplifier drive circuits 57 are removed from each row 104 of back layer connecting regions 44, to be replaced by sense amplifier drive circuits 57' each of which is contained within a region in which a sense amplifier circuit 6 is formed. In addition, each of these sense amplifier drive circuits 57' does not include an inverter, and instead, an inverted signal of the sense amplifier activation line 43 is supplied to these in common from the output of a first-stage inverter within the sense amplifier drive circuit 58, as shown. Thus by comparison with the first embodiment, this embodiment may enable the width of each row region 104 of back layer connecting regions 44 to be reduced, thereby enabling an even higher degree of integration. Otherwise, the results that are obtained by this embodiment are similar to those obtained for the first embodiment, as described above.

A third embodiment of the present invention will be described referring to FIG. 8. This embodiment differs from the first embodiment of FIG. 6 in that a stabilizing capacitor 71 is formed within each region in which a sense amplifier circuit 6 is formed, connected between the V_{SS} and V_{DD} supply potentials, more specifically, connected between two adjacent lines of the Vss supply mesh 110 and the Vdd supply mesh 120. In addition, a stabilizing capacitor 72 is connected between two adjacent lines of the Vss supply mesh 110 and Vdd supply mesh 120 within each row 104 of back layer connecting regions 44. These capacitors augment the naturally occurring stray capacitances between the Vss supply mesh 110 and Vdd supply mesh 120, and serve to prevent noise and crosstalk voltages from being conveyed by these power supply meshes, i.e. provide increased voltage stability for the Vss supply mesh 110 and Vdd supply mesh 120. Alternatively stated, for a given degree of voltage stability of the Vss supply mesh 110 and Vdd supply mesh 120, the line widths of these can be made narrower by incorporating the capacitors 71, 72, so that the overall area occupied by connecting lines can be reduced.

Moreover, the sum of the capacitances of these capacitors 71 and 72 will constitute a substantially large capacitance value in the overall memory chip, so that these are extremely effective in stabilizing the values of supply voltages V_{DD} and V_{SS} that are applied to peripheral circuits of the chip, and hence the overall operation of the semiconductor memory is further stabilized.

In the above, it is assumed that the capacitors 71, 72 are respectively provided within each sense amplifier circuit 6 region and also within each back layer connecting region region (between each pair of adjacent columns of memory cell regions). However it would be equally possible to provide such a capacitor only within each sense amplifier circuit 6 region, or to form the capacitors only within each row 104 of back layer connecting regions 44 (between each pair of adjacent regions 44).

A fourth embodiment of the present invention will be described referring to FIG. 9. This differs from the second embodiment described hereinabove in that the stabilization capacitors 71, 72 of the third embodiment are further incorporated. The results obtained are similar to those obtained by the third embodiment.

In each of the first through fourth embodiments of the present invention described above, an n-channel MOS transistor 62 is used in each sense amplifier drive circuit 57 as a sense amplifier drive transistor for driving the p-channel FFs of the sense amplifier circuits 6 via the sense amplifier p-channel FF drive line 8. However as mentioned hereinabove, it would be equally possible to use a p-channel MOS transistor for that purpose. FIG. 10A shows a first example of an alternative circuit for the sense amplifier drive circuit 57, in which a p-channel MOS transistor 162 is used in place of the p-channel MOS transistor 62, while also inserting an additional inverter 163 in each sense amplifier drive circuit 57, for driving the gate of the p-channel MOS transistor 162. FIG. 10B shows a second alternative configuration for the sense amplifier drive circuit 57. In this case, the gate of the p-channel MOS transistor 162 is driven directly from the sense amplifier activation line 43, which is connected in common to a column of sense amplifier drive circuits 57.

It can be understood from the above description that a semiconductor memory apparatus according to the present invention provides significant advantages over the prior art, with respect to enabling a higher degree of component integration to be achieved in order to produce a dynamic random access memory having increased storage capacity, which does not have an increased degree of read access time by comparison with prior art DRAMs having a lower storage capacity. That advantage is achieved by providing two voltage supply meshes which extend throughout a memory array region in which memory cells are formed, thereby enabling sense amplifier drive circuits (which drive the sense amplifier circuits of these memory cells) to be distributed throughout that region, by enabling each of the sense amplifier drive circuits to be directly coupled to receive supply voltages from immediately adjacent points on the respective meshes, i.e. ensuring in effect that each sense amplifier drive circuits is connected directly to a low-impedance drive voltage source, even if the sense amplifier drive circuit is located at a distance from the periphery of the memory array region.

What is claimed is:

1. A semiconductor memory apparatus including a memory array region having formed therein:

a plurality of unit memory cell blocks distributed through said memory array region at regular spacings, each formed of an array of memory cells;

a plurality of unit sense amplifier blocks distributed among said unit memory cell blocks at regular spacings, each formed of an array of sense amplifier circuits;

a plurality of sense amplifier drive circuits for driving said sense amplifier circuits, distributed among said unit sense amplifier blocks at regular spacings; and

first and second voltage supply meshes, mutually electrically isolated and each extending throughout said memory array region, respectively coupled to receive first and second supply voltages;

each of said sense amplifier drive circuits being coupled to an adjacent point on said first voltage supply mesh to receive said first supply voltage and to an adjacent point on said second voltage supply mesh to receive said second supply voltage.

2. A semiconductor memory apparatus according to claim 1, in which each of said said first and second voltage supply meshes is formed of a plurality of first supply lines extending in a first direction and formed in an upper layer of a substrate of said semiconductor memory apparatus and a plurality of second supply lines extending in a second direction and formed in a lower layer of said substrate which is electrically isolated from said upper layer, and a plurality of through-hole connections for interconnecting said first and second supply lines at points of intersection thereof.

3. A semiconductor memory apparatus according to claim 2, in which each of said first and second supply lines of said first voltage supply mesh is connected to said first supply voltage by at least one end thereof, and in which each of said first and second supply lines of said second voltage supply mesh is connected to said second supply voltage by at least one end thereof.

4. A semiconductor memory apparatus according to claim 1, in which each of said sense amplifier drive circuits is formed within a portion of said memory array region in which is formed one of said sense amplifier circuits.

5. A semiconductor memory apparatus according to claim 1, further comprising a plurality of voltage stabilizing capacitors each formed within a portion of said memory array region in which is formed one of said sense amplifier circuits.

6. A semiconductor memory apparatus according to claim 1, in which said plurality of unit memory cell blocks are configured as a plurality of columns of unit memory cell blocks each extending in a first direction, each column consisting of a plurality of said unit memory cell blocks disposed at regular spacings, and in which each of said memory cells is connected to one of a plurality of word lines which extend in said first direction, each of said word lines being formed of an upper conductor formed in an upper layer of a substrate of said semiconductor memory apparatus and a lower conductor formed in a lower layer of said substrate, said upper and lower conductors being interconnected by through-hole connections in each of a plurality of connection regions provided at intervals throughout each of said columns.

7. A semiconductor memory apparatus according to claim 6, in which each of said sense amplifier drive circuits is disposed in a region between two adjacent ones of said connection regions of two adjacent ones of said columns.

8. A semiconductor memory apparatus according to claim 6, further comprising a plurality of voltage stabilizing capacitors each connected between said first and second voltage supply meshes and disposed within a region between two adjacent ones of said connection regions of two adjacent ones of said columns.

9. A semiconductor memory apparatus according to claim 8, further comprising a plurality of voltage stabilizing capacitors each formed within a portion of said memory array region in which is formed one of said sense amplifier circuits.

* * * * *

EXHIBIT 2

United States Patent [19]

Kannan et al.

[11] **Patent Number: 5,053,998**

[45] **Date of Patent: Oct. 1, 1991**

[54] **SEMICONDUCTOR MEMORY DEVICE WITH DUAL DRIVERS TO SENSE AMP ARRAY**

[75] Inventors: **Yasushi Kannan**, Otokuni; **Takashi Taniguchi**, Moriguchi; **Michiharu Shikata**, Kusatsu; **Tatsumi Sumi**, Mishima, all of Japan

[73] Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka, Japan

[21] Appl. No.: **493,686**

[22] Filed: **Mar. 15, 1990**

[30] **Foreign Application Priority Data**

Mar. 15, 1989 [JP] Japan 1-67079

[51] **Int. Cl.**[5] **G11C 7/00**

[52] **U.S. Cl.** **365/194**; 365/154; 365/205; 365/208; 365/287; 365/233

[58] **Field of Search** 365/227, 205, 207, 208, 365/233, 194, 154

[56] **References Cited**

U.S. PATENT DOCUMENTS

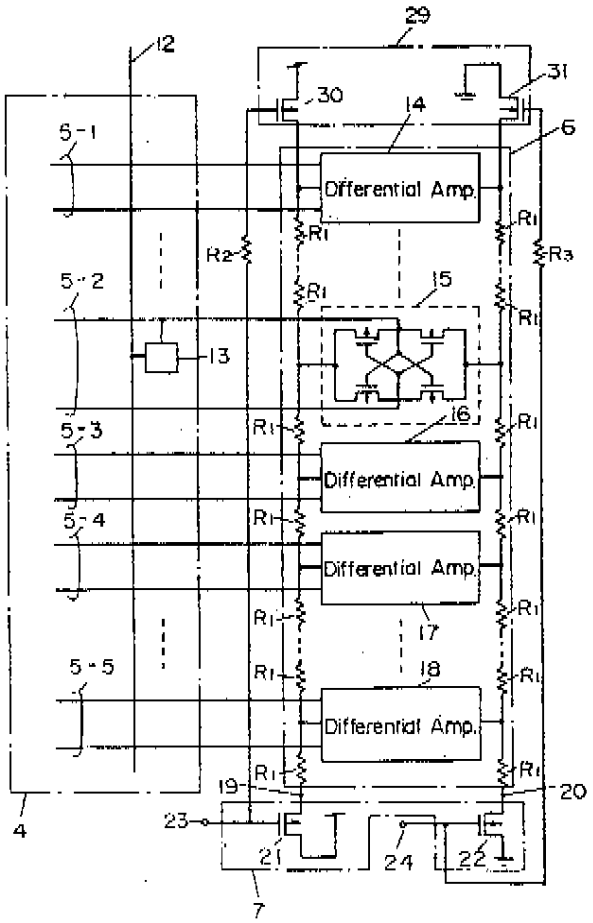
4,916,671 4/1990 Ichiguchi 365/207

Primary Examiner—Joseph E. Clawson, Jr.
Attorney, Agent, or Firm—Wenderoth, Lind & Ponack

[57] **ABSTRACT**

A sense amplifier is driven by two sense amplifier drivers which operate at a different timing from each other. This can prevent the increase of the peak value of an instantaneous current in the operation of the plurality of differential amplifiers, thus resulting in ensuring that the potential of the signal line connected to the sense amplifier will be changed in a rapid manner. This may bring about a solution of the problem of the delay in timing of starting of specific differential amplifiers so as to enable correct data to be transmitted to the next circuit at all times. Furthermore, by connecting the sense amplifier drivers to opposite ends of the restore and drive signal lines, respectively, the wiring resistance of the restore and drive signal lines may be substantially reduced, thereby improving precise high speed data transmission.

9 Claims, 9 Drawing Sheets



a means for reading into a plurality of data lines data from said plurality of memory cells in said memory cell array;

sense amplifiers consisting of a plurality of differential amplifiers for amplifying data read into said plurality of data lines;

a plurality of sense amplifier drivers connected to a plurality of positions of the signal lines respectively which are in turn connected in common to said plurality of differential amplifiers, and

a means for giving a time difference to the operation starting timing of said plurality of sense amplifier drivers.

8. A semiconductor memory device as defined in claim 7, wherein said delay means is constituted by the wiring resistance and parasitic capacitance of said signal lines.

9. A semiconductor memory device as defined in claim 7, wherein said delay means is constituted by the wiring resistance and parasitic capacitance of said signal lines, and an inverter circuit means connected to said signal lines.

* * * * *

EXHIBIT 3

US005475648A

United States Patent [19]

Fujiwara

[11] Patent Number: 5,475,648

[45] Date of Patent: Dec. 12, 1995

[54] **REDUNDANCY SEMICONDUCTOR MEMORY DEVICE WHICH UTILIZES SPARE MEMORY CELLS FROM A PLURALITY OF DIFFERENT MEMORY BLOCKS, AND UTILIZES THE SAME DECODE LINES FOR BOTH THE PRIMARY AND SPARE MEMORY CELLS**

[75] Inventor: **Atsushi Fujiwara**, Kyoto, Japan

[73] Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka, Japan

[21] Appl. No.: **13,382**

[22] Filed: **Feb. 4, 1993**

[30] **Foreign Application Priority Data**

Feb. 7, 1992 [JP] Japan 4-022298

[51] **Int. Cl.**[6] **G11C 7/00**

[52] **U.S. Cl.** **365/230.06**; 365/200; 365/230.03; 371/10.3

[58] **Field of Search** 365/200, 230.03, 365/225.7, 230.06; 371/10.2, 10.3, 10.1

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,656,610	4/1987	Yoshida et al.	365/200
4,860,260	8/1989	Saito et al.	365/201
4,908,798	3/1990	Urai	365/230.03
5,021,944	6/1991	Sasaki et al.	365/200
5,126,973	6/1992	Gallia et al.	365/200
5,224,073	6/1993	Nakayama	365/200
5,243,570	9/1993	Saruwatari	365/201
5,255,227	10/1993	Haelfele	365/200
5,257,229	10/1993	McClure et al.	365/200
5,270,976	12/1993	Tran	365/200
5,295,101	3/1994	Stephens, Jr. et al.	365/200
5,307,316	4/1994	Takemae	365/200

FOREIGN PATENT DOCUMENTS

62-125598	6/1987	Japan .
1-112598	5/1989	Japan .
2-113490	4/1990	Japan .

Primary Examiner—David C. Nelms
Assistant Examiner—Andrew Q. Tran
Attorney, Agent, or Firm - Willian Brinks Hofer Gilson & Lione

[57] **ABSTRACT**

A semiconductor memory device with a redundancy configuration with a higher corrective efficiency is disclosed. Primary memory cell arrays 3*a*, 3*b*, and 3*c* are arranged in memory cell blocks a, b, and c. Spare memory cell arrays 2*b* and 2*c* are arranged in the memory cell blocks b and c. When the address of an address signal supplied agrees with the address of a defective primary memory cell in one memory cell block, a spare memory cell in the other memory cell block selected for such a defective memory cell. Even if a word line of the primary and a word line of the spare memory cells are selected at the same time, it is possible to access read data in a nondestructive manner. This achieves a high-speed word line activation as well as an improved corrective efficiency. The provision of a row decoder that connects a primary word line to a spare word line with a shared decode line prevents the increase of the area of memory chips due to the arrangement of a spare memory cell.

9 Claims, 11 Drawing Sheets

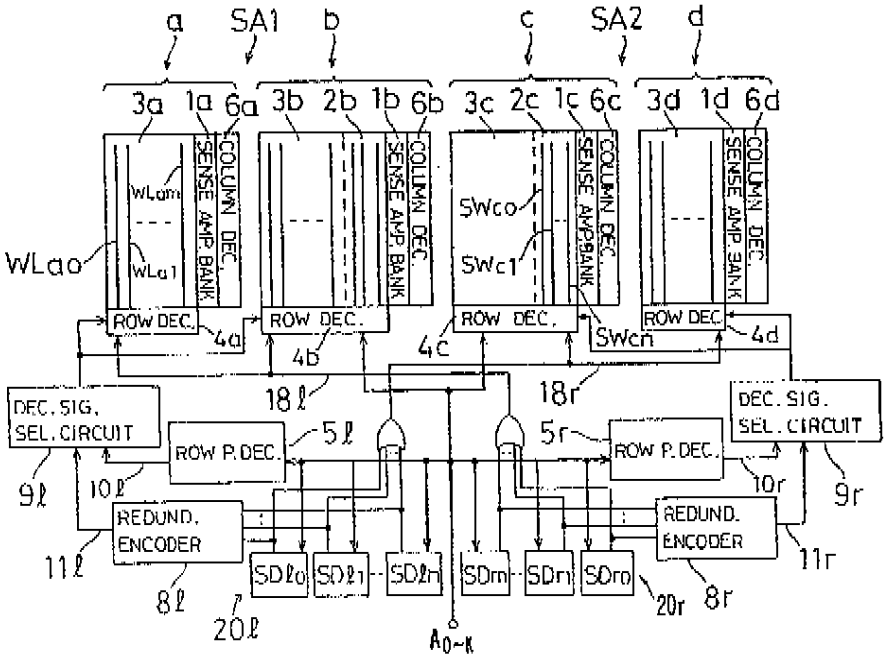


FIG. 1

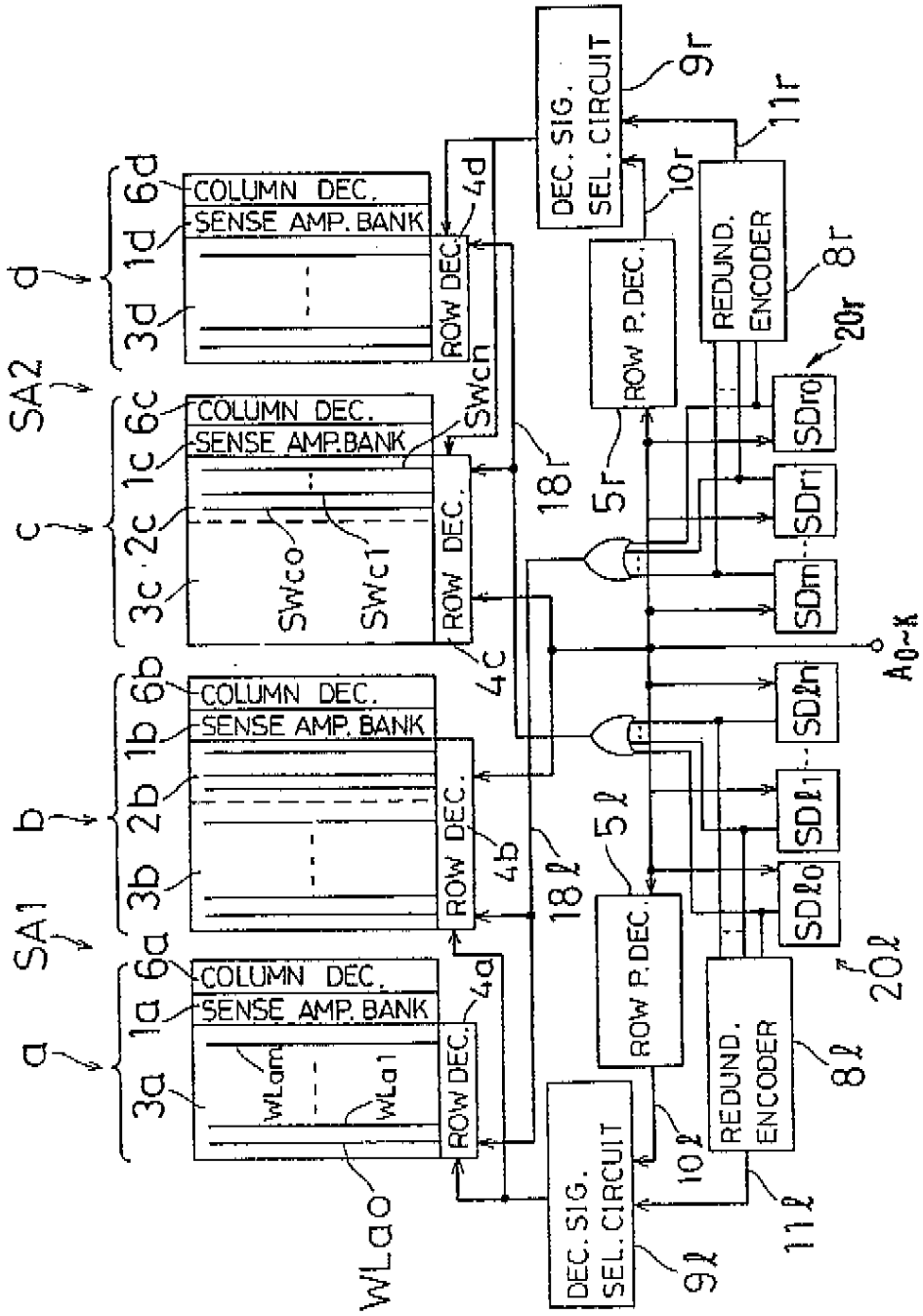

COLUMN DEC.
SENSE AMP. BANK
ROW DEC.
SWco
SWc1
SWcn
WLa0
WLa1
WLam
DEC. SIG. SEL. CIRCUIT
ROW P. DEC.
REDUND. ENCODER
SDr0
SDr1
SDrn
SDl0
SDl1
SDln
A0~k
SA1
SA2
a
b
c
d

FIG. 2

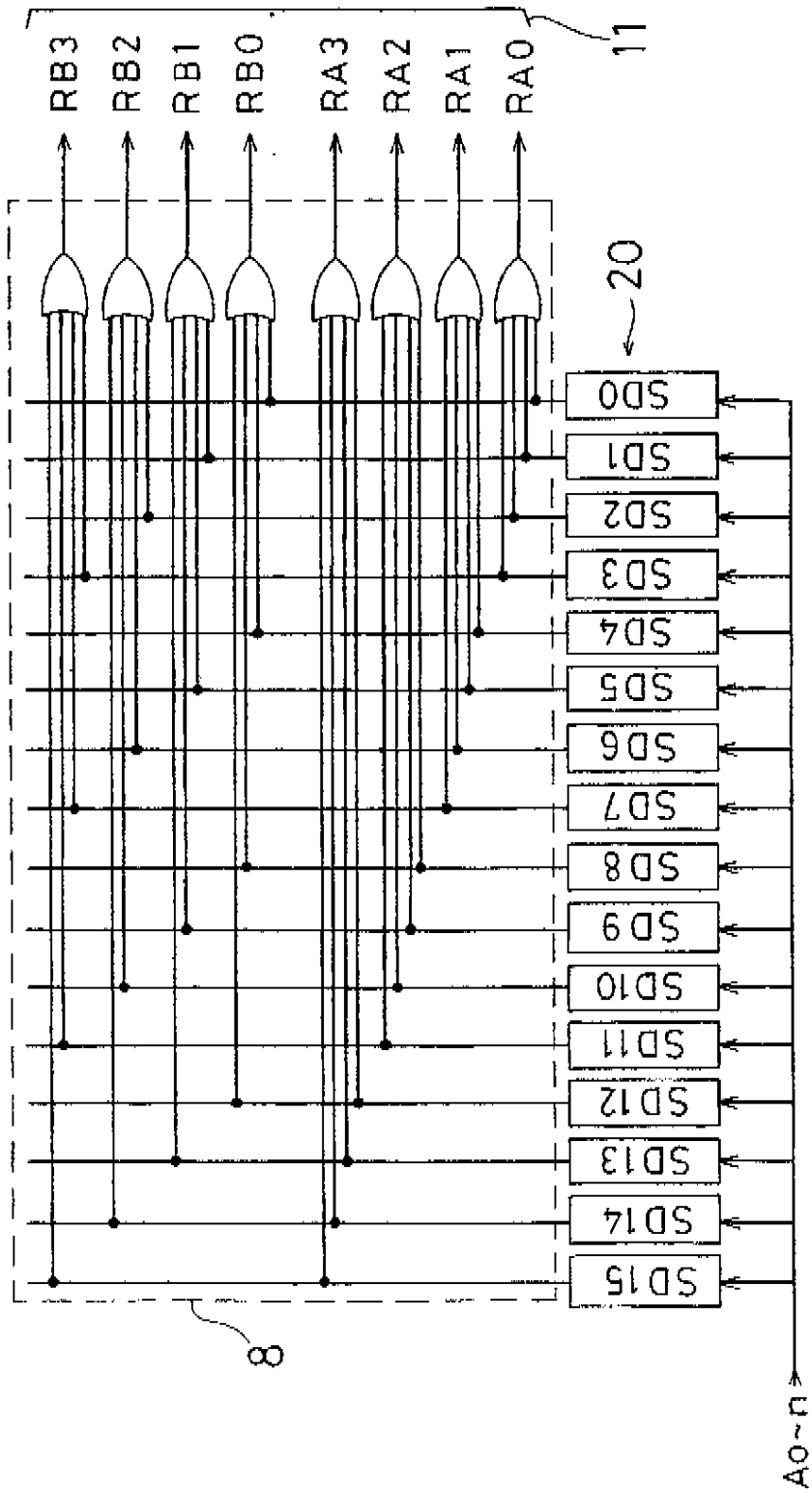
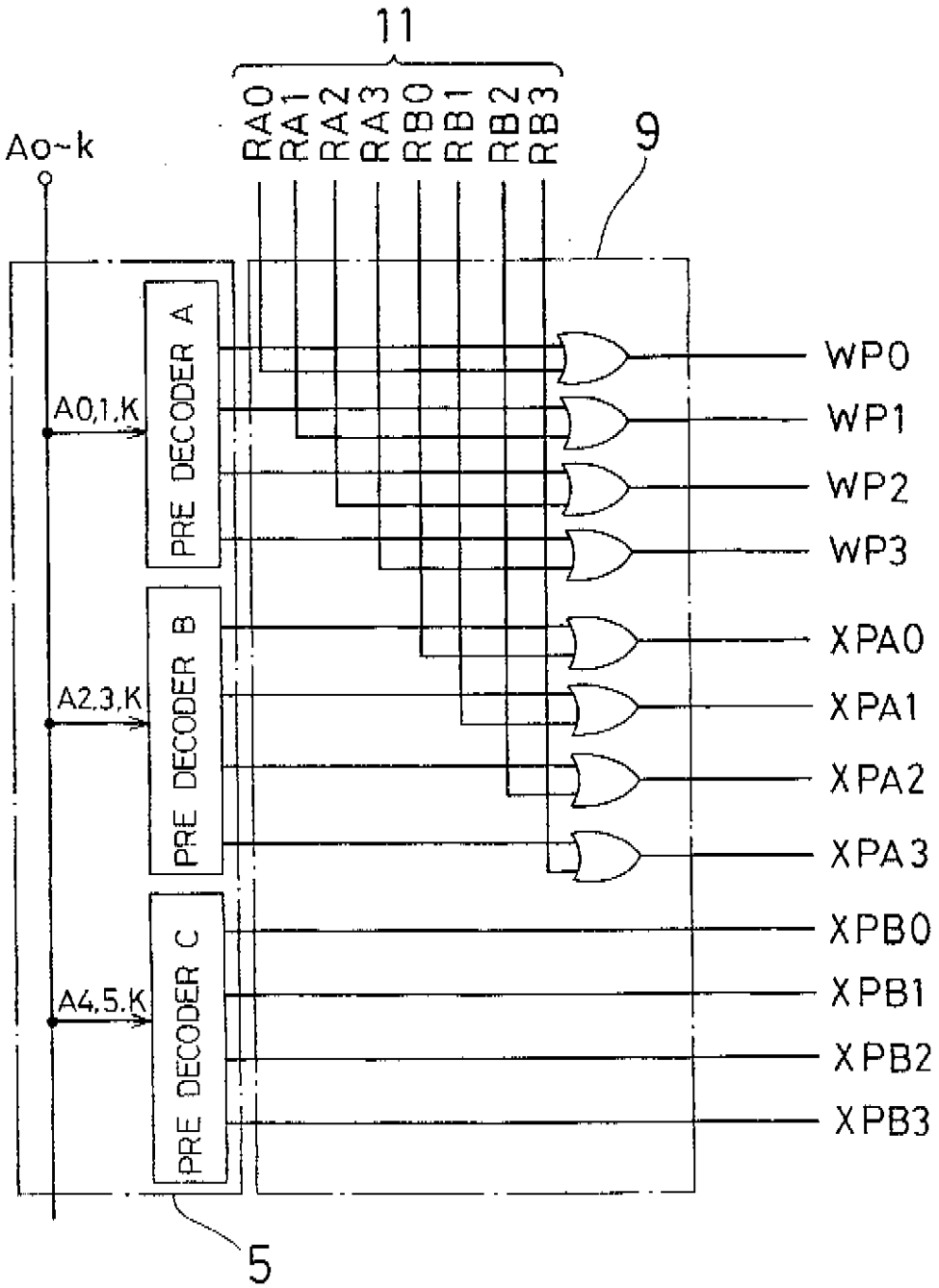

RB3
RB2
RB1
RB0
RA3
RA2
RA1
RA0
11
20
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
8
A0~n

FIG. 3


11
RA0
RA1
RA2
RA3
RB0
RB1
RB2
RB3
9
Ao~k
A0,1,K
A2,3,K
A4,5,K
PRE DECODER A
PRE DECODER B
PRE DECODER C
WP0
WP1
WP2
WP3
XPA0
XPA1
XPA2
XPA3
XPB0
XPB1
XPB2
XPB3
5

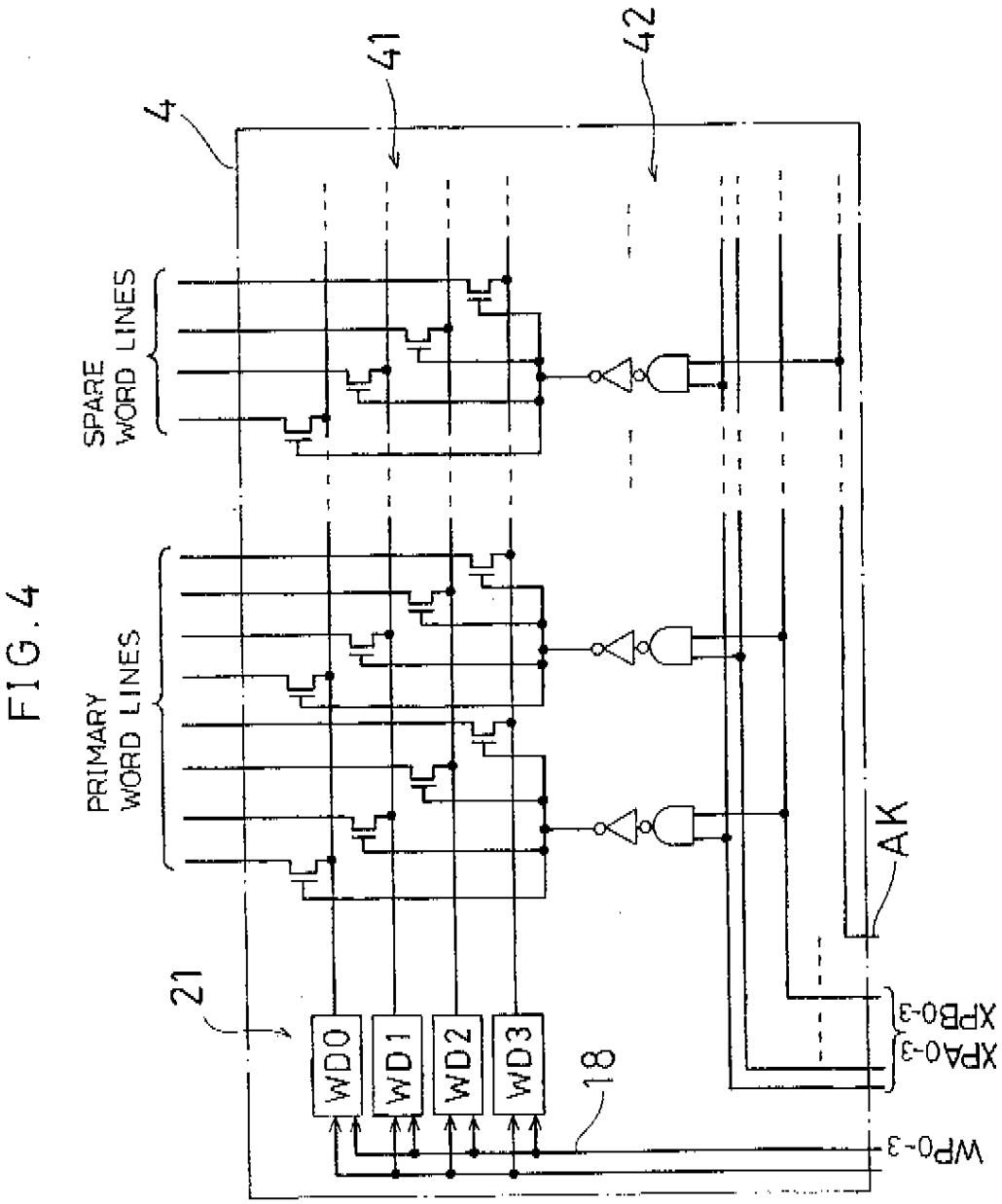

4
41
42
SPARE WORD LINES
PRIMARY WORD LINES
AK
21
WD0
WD1
WD2
WD3
18
XPB0-3
XPA0-3
WP0-3

FIG. 4

FIG.5

(a) PRIOR ART

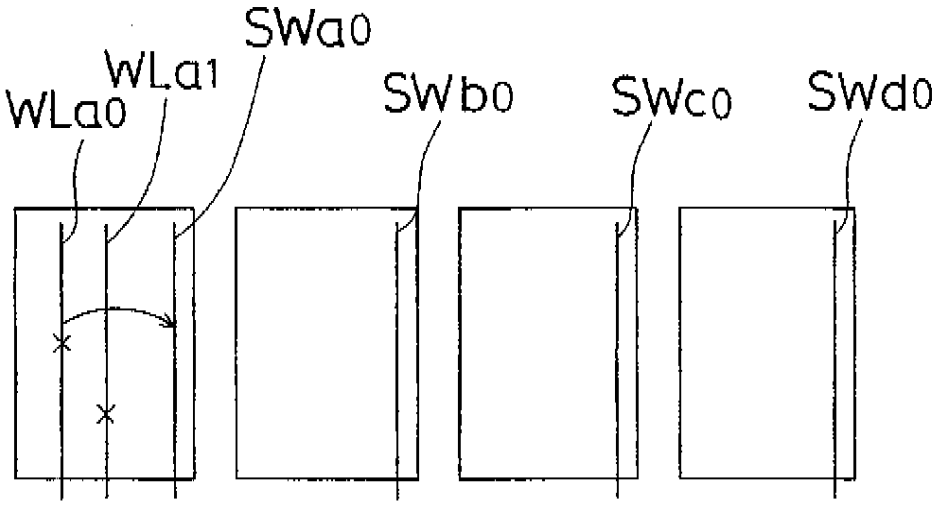


FIG.5

(b) PRESENT INVENTION

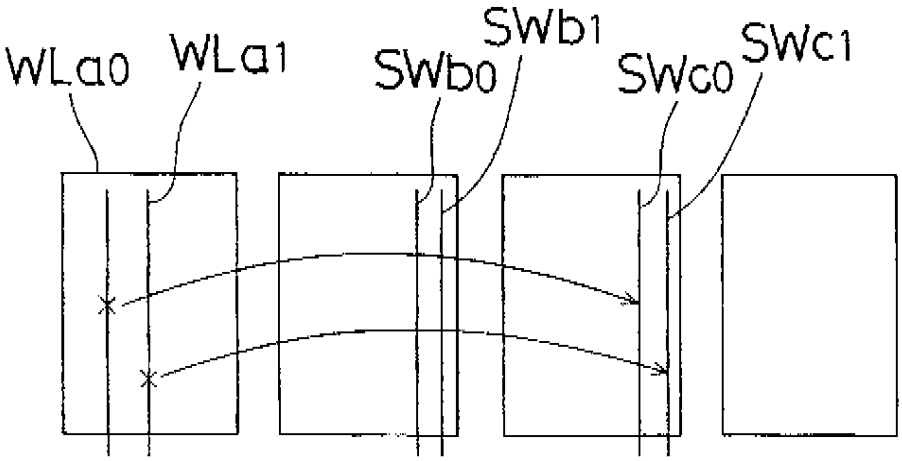


FIG. 6

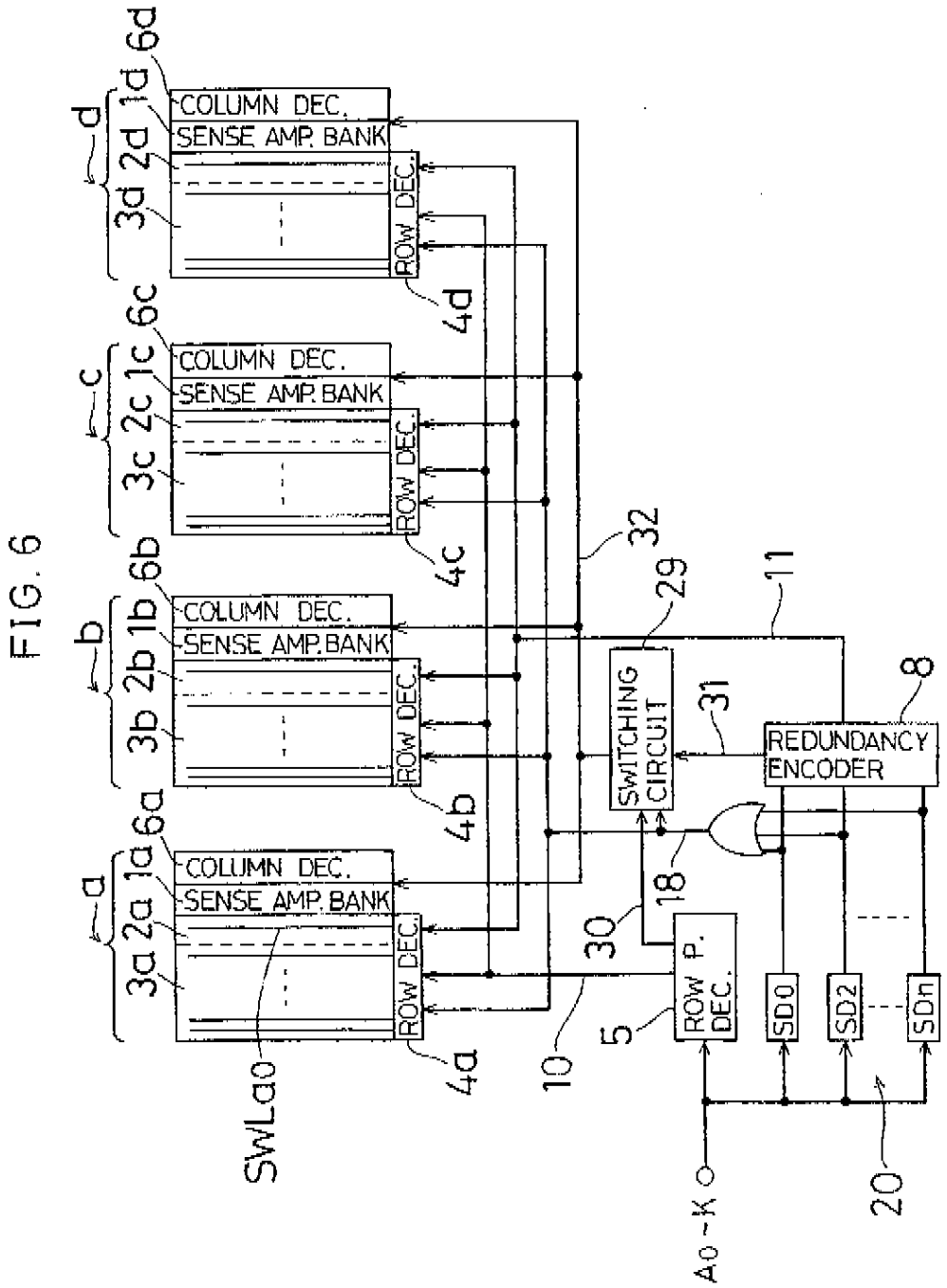

COLUMN DEC.
SENSE AMP. BANK
ROW DEC.
SWITCHING CIRCUIT
REDUNDANCY ENCODER
ROW P. DEC.
SD0
SD2
SDn
SWLa0
A0~K
a
b
c
d
1a
1b
1c
1d
2a
2b
2c
2d
3a
3b
3c
3d
4a
4b
4c
4d
5
6a
6b
6c
6d
8
10
11
18
20
29
30
31
32

FIG. 7

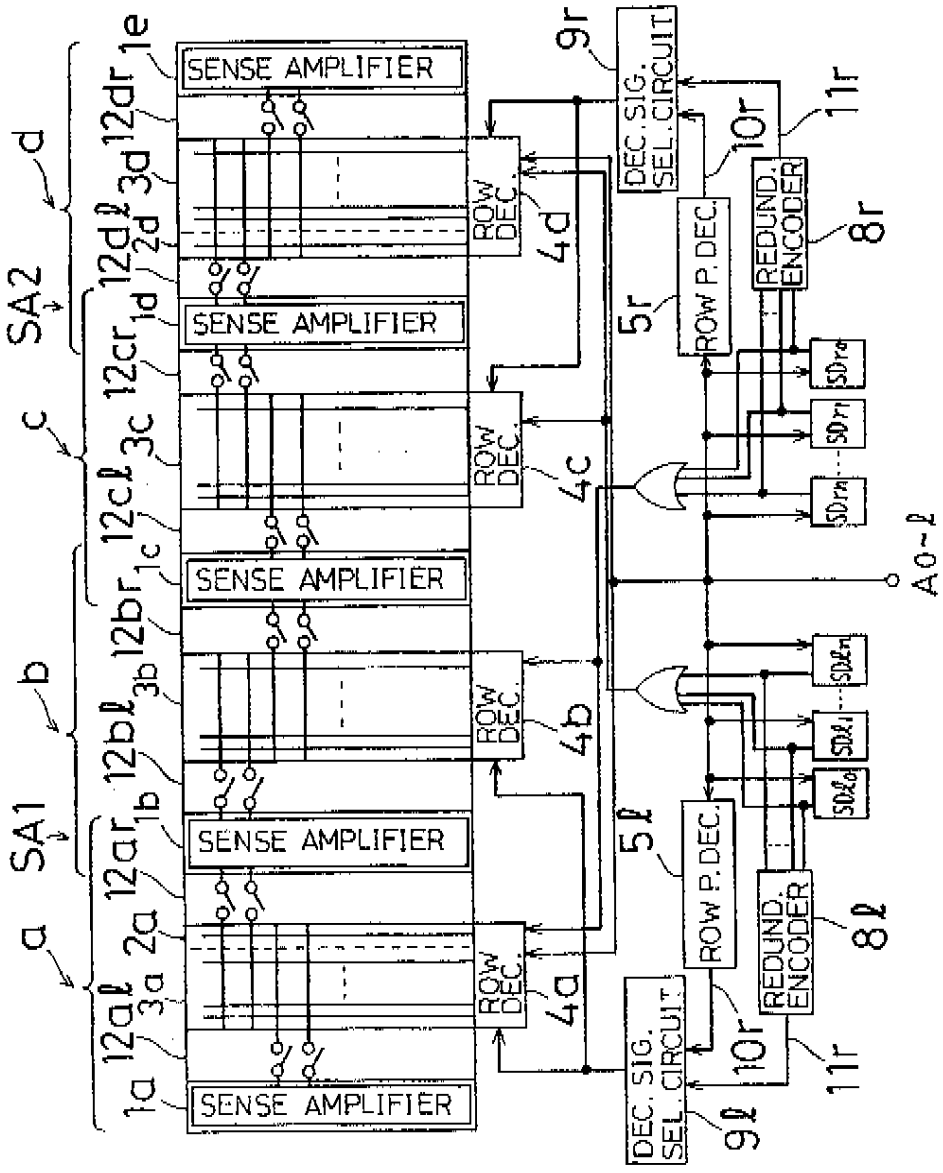

SENSE AMPLIFIER
ROW DEC.
DEC. SIG. SEL. CIRCUIT
ROW P. DEC.
REDUND. ENCODER
SA1
SA2
a
b
c
d
A0~l

FIG.8

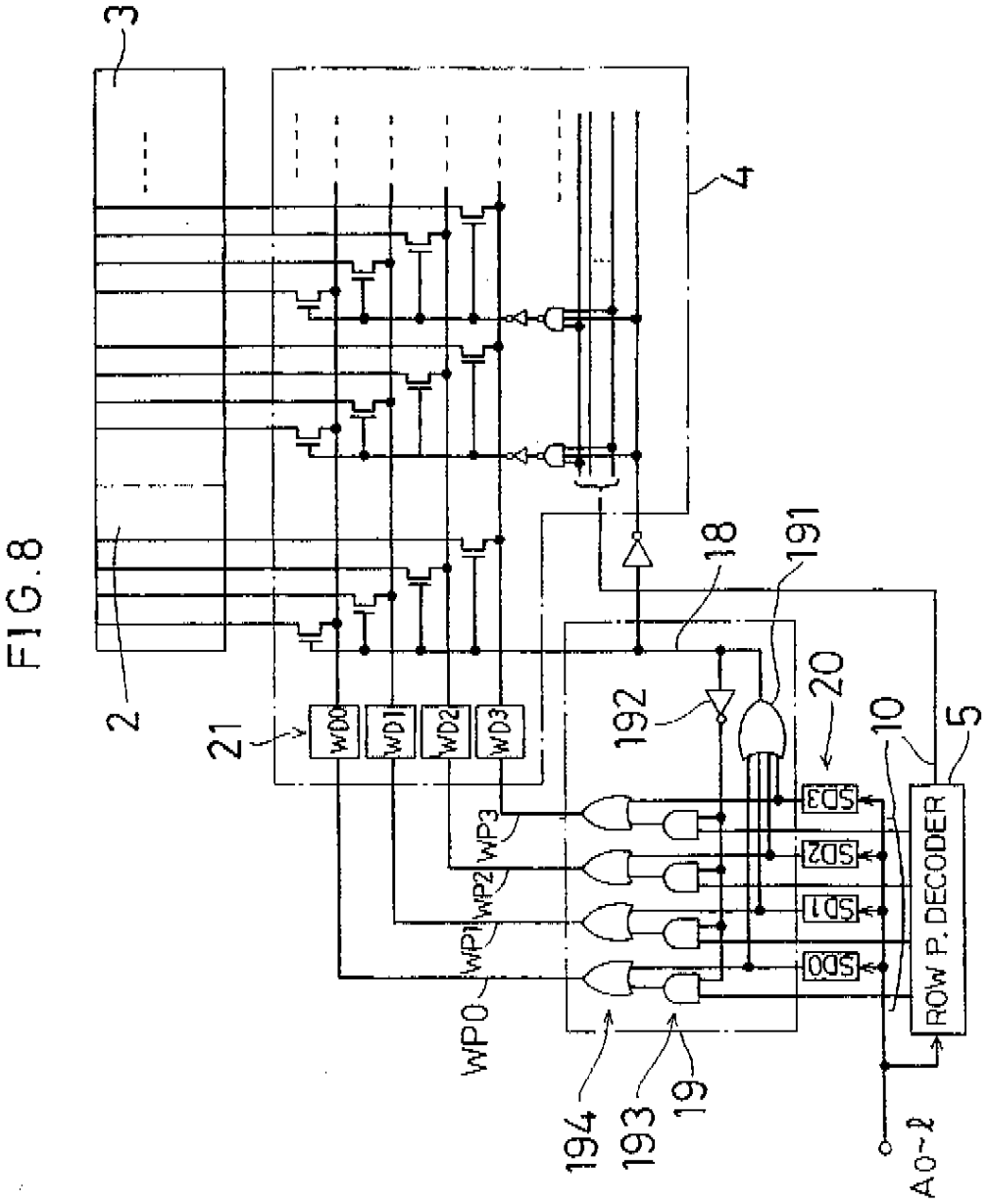
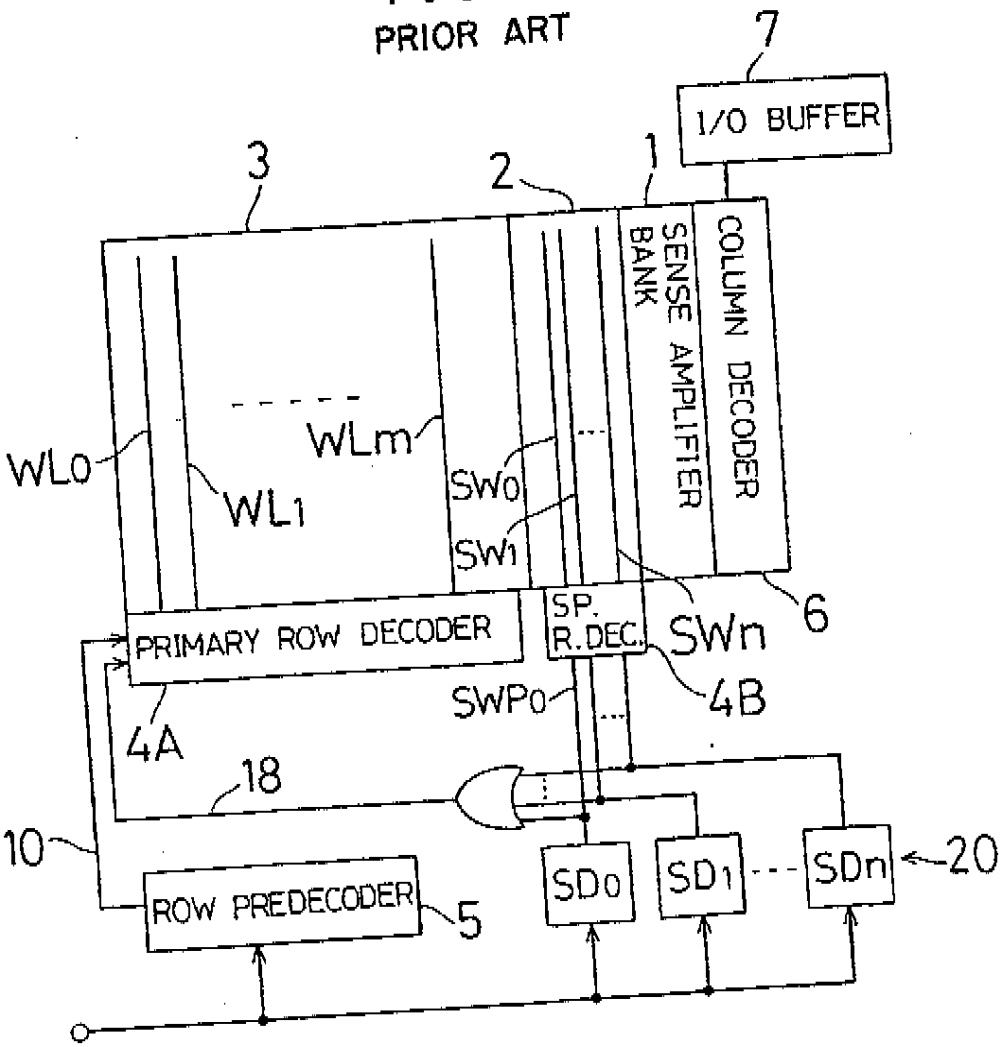

3
4
2
21
WD0
WD1
WD2
WD3
18
191
192
20
10
5
SD3
SD2
SD1
SD0
ROW P. DECODER
WP3
WP2
WP1
WP0
194
193
19
A0~2

FIG. 9
PRIOR ART



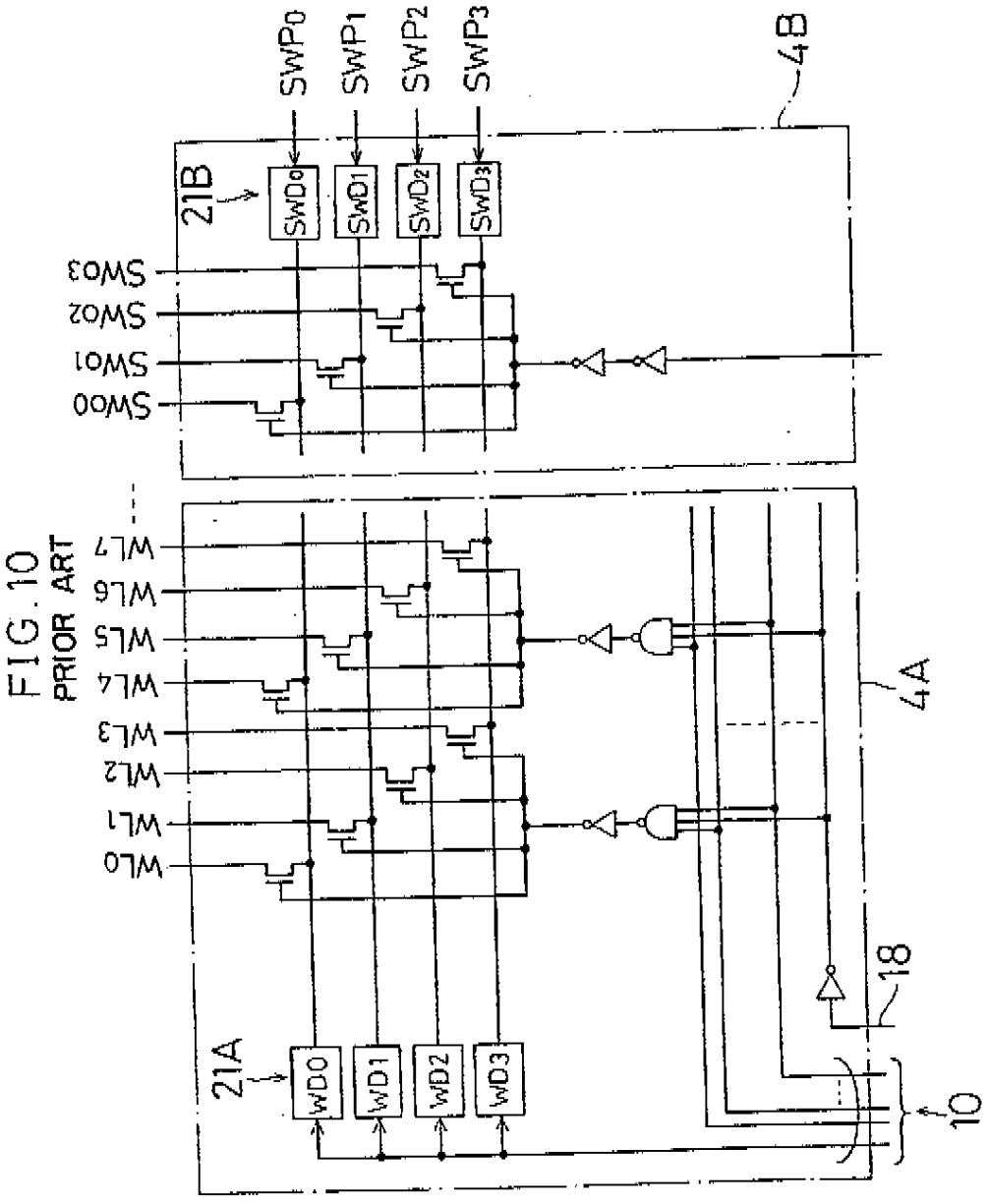


FIG. 10
PRIOR ART

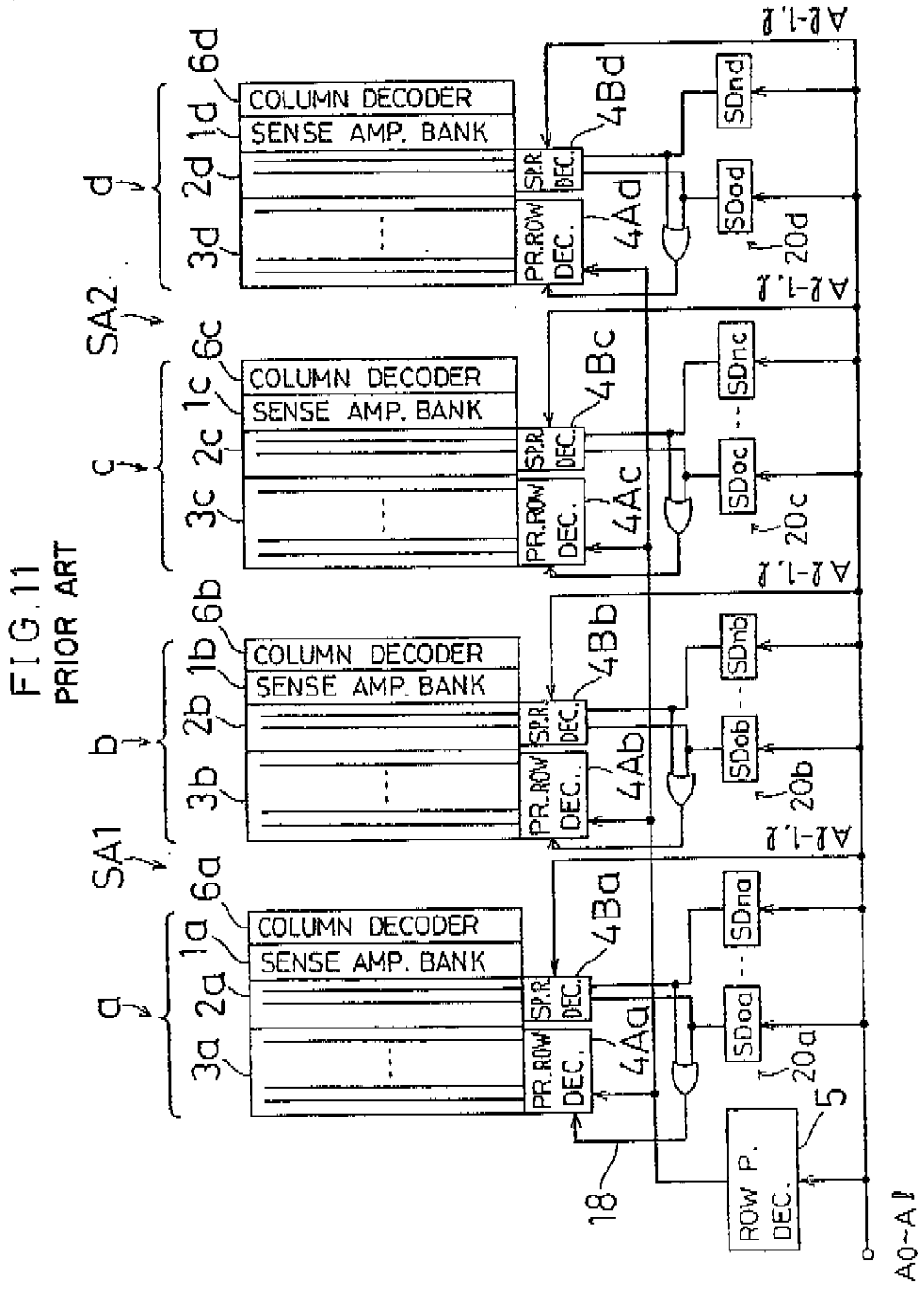


FIG. 11
PRIOR ART

REDUNDANCY SEMICONDUCTOR MEMORY DEVICE WHICH UTILIZES SPARE MEMORY CELLS FROM A PLURALITY OF DIFFERENT MEMORY BLOCKS, AND UTILIZES THE SAME DECODE LINES FOR BOTH THE PRIMARY AND SPARE MEMORY CELLS

BACKGROUND OF THE INVENTION

This invention relates to an improvement in semiconductor memory devices with a redundant configuration to electrically provide a corrective for defective bits.

The storage capacity of semiconductor memory devices has been increased. The number of components per memory chip has been increased. The area of the memory chip has been increased. If only defect-free memory chips are selectively used, this presents a disadvantage to manufacturing costs. This calls for a corrective technique with respect to a defective bit. It is known that a semiconductor memory device employs therein a redundant configuration in which besides a primary memory cell a spare memory cell is provided so that the spare memory cell will take over from the primary memory cell in the event of failure. Following the fabrication of the semiconductor memory device, primary memory cells are first checked for possible defect. Then, if a defective primary memory cell is found, it is replaced by a spare memory cell. Thus, storage capacitance to be achieved is satisfied.

A semiconductor memory device incorporating therein the foregoing redundant configuration is known from Japanese Patent Application, published under No. 1-112598. In accordance with this semiconductor memory device, primary memory cells and spare memory cells (i.e., defect corrective memory cells) are organized in a matrix structure to form a memory cell array, and the primary memory cells are interconnected through word lines and bit lines while on the other the spare memory cells are connected together either with word lines or with bit lines, or with both the word and bit lines. The address of a defective primary memory cell is replaced by the address of a spare memory cell so that the defective memory cell is corrected. Japanese Patent Application, published under No. 62-125598, discloses a technique in which a first decoder circuit to select primary memory cells and a second decoder circuit to select spare memory cells are provided. The first decoder circuit is so organized that a plurality of logical circuits of current switching type are longitudinally stacked. During the defect corrective, a non-selective pulse voltage and a selective pulse voltage are applied to the first decoder circuit and the second decoder circuit respectively, making a defective primary memory cell non-selective and a spare memory cell selective at the same time. Additionally, U.S. Pat. No. 4,860,260, JP Patent Application, published under No. 2-113490, and JP Patent Application, published under No. 57-111893 disclose semiconductor memory devices incorporating a redundant configuration.

FIG. **9** illustrates a typical redundant configuration incorporated in the above-described conventional semiconductor memory device. Such a redundant configuration contains a sense amplifier array **1**, a spare memory cell array **2**, a primary (main) memory cell array **3**, a primary row decoder **4**A, a spare row decoder 4B, a row predecoder **5**, a redundancy-use decision circuit **20**, comprised of elements SD0 to SDn to store the addresses of defective memory cells and to decide whether an input address corresponds to the stored address, a column decoder **6**, a data I/O buffer **7**, and word lines WL0 to WLm of the primary memory cell array **3**. Spare word lines of the spare memory cell array **2**, indicated by SW0 to SWn, are selected by a signal from the redundancy-use decision circuit **20**.

FIG. **10** shows how the primary row decoder **4**A and the spare row decoder **4**B are organized.

The operation of a memory readout in correcting a defective memory cell is now described. Here, it is assumed that the primary word line WL0 of the primary memory cell contains a defective memory cell, and that the word line WL0 is replaced by the spare word line SL0 of the spare memory cell.

When ADDRESS SIGNALS A0 to A1 are fed to the row predecoder **5** as well as to the redundancy-use decision circuit **20**, the elements SD0 to SDn of the decision circuit **20** each make a comparison between the addresses of ADDRESS SIGNALS A0 to A1 supplied and their stored addresses of the defective memory cells. For example, if ADDRESS SIGNAL supplied happens to be an address corresponding to the primary word line WL0 of the primary memory cell array **3**, this means that the address stored in the element SD0 of the decision circuit **20** agrees with the address of supplied ADDRESS SIGNAL. Then, REDUNDANCY-USE SIGNAL is sent out from the element SD0 of the redundancy-use decision circuit **20**. This REDUNDANCY-USE SIGNAL is fed to the primary row decoder **4**A as PRIMARY MEMORY STOP SIGNAL **18**. Upon receiving STOP SIGNAL **18**, the primary row decoder **4**A stops operating thereby making the primary word line WL0 non-selective. REDUNDANCY-USE SIGNAL is also supplied to the spare row decoder **4**B as REDUNDANCY-SELECTION SIGNAL SWP0 to select the spare word line SW0. This replaces the primary word line WL0 containing the defective memory cell with the spare word line SW0. In this way, the defective memory cell can be corrected.

Next, a conventional semiconductor memory device in which a plurality of memory cells are zoned to form memory cell blocks is described, which is shown in FIG. **11**. In accordance with this semiconductor memory device, a memory cell block a (b, c, d) contains a sense amplifier array **1**a (**1***b*, 1c, **1***d*), a spare memory cell array **2***a* (**2***b*, **2***c*, **2***d*), a primary memory cell array **3***a* (**3***b*, **3***c*, **3***d*), a column decoder **6***a* (**6***b*, **6***c*, **6***d*), a primary row decoder **4**A*a* (**4**A*b*, 4A*c*, **4**A*d*), a redundancy signal generating circuit **20***a* comprised of elements SDoa to SDna (**20***b* comprised of elements SDob to SDnb, **20***c* comprised of SDoc to SDnc, and **20***d* comprised of elements SDod to SDnd), and a row predecoder **5** that is shared among the memory cell blocks. Only one of the memory cell blocks a, b, c, and d is selected by A1 - **1**,1 of supplied ADDRESS SIGNALS A0 to A1 and is brought into operation. The operation of the memory cell blocks a, b, c, and d is the same as the one described in FIG. **8**.

Both the conventional semiconductor memory devices of FIG. **9** and FIG. **11**, however, require the provision of word lines for every memory cell block. Further, if a defective memory cell is found in a memory cell block, only a spare word line (i.e., a spare memory cell), arranged in the same memory cell block that the defective memory cell is contained, can provide a corrective for the defective memory cell. The size of memory increases with the number of memory cell blocks. This causes the number of spare word lines to increase in a memory chip. As component density per memory chip becomes higher, more complicated fabrication technique is required. Not only the number of spare

word lines necessary for a single memory cell block, but also the number of decode lines used to select a spare word line increases. As the number of spare word lines increases, a greater chip area is required.

As the scale of integration becomes larger, the layout pitch of row decoders gets narrower. In order to reduce the pitch, one row decoder is provided for a plurality of word lines, and the word lines are selected by WORD LINE DRIVE SIGNAL, as shown in FIG. **10**. In order to drive the spare word lines, the conventional semiconductor memory device additionally requires, besides a primary word line drive signal generation circuit 21A comprised of elements **WD0** to WD3, a spare word line drive signal generating circuit 21B comprised of elements SWD0 to SWD3 corresponding to spare word lines SWo0 to SWo3. In this example, however, the spare word line drive signal generating circuit 21B requires four elements (i.e., the elements SWD0 to SWD3), since four spare word lines are provided. The number of spare word lines increases with the scale of integration, which presents a problem that the area of the memory chip disadvantageously increases.

SUMMARY OF THE INVENTION

Bearing the foregoing problems in mind, the present invention was made. It is a general object of the invention to improve the efficiency of corrective and to prevent the chip area from increasing due to the layout of the spare memory cell by making, even in cases where a defective memory cell occurs in one memory cell array that has no spare memory cells left, a spare memory cell in the other memory cell array available.

To accomplish the foregoing objects, the present invention proposes the following means.

A first means provides a semiconductor memory device which comprises a plurality of memory cell blocks each containing a plurality of memory cells, wherein: of the memory cells certain plural memory cells and all other plural memory cells are arranged so that the former memory cells serve as primary memory cells and the latter memory cells on the other hand serve as spare memory cells; and memory replacement means is provided which stores the address of a defective primary memory cell in one of the memory cell blocks and selects, when the address of an address signal supplied agrees with the address of a defective memory cell, a spare memory cell in the other memory cell block for the defective primary memory cell. Therefore, the defective memory cell corrective efficiency can be improved since a defective memory cell in one memory cell block can be replaced by a spare memory cell in the other memory cell block.

A second means provides a semiconductor memory device, wherein the memory replacement means is organized so that it can select a spare memory cell from a memory cell block containing therein a defective primary memory cell. Therefore, the spare memory cell availability can be improved since, when all spare memory cells in one memory cell block are used up, other spare memory cells in the other memory cell block become ready for further defective memory cell corrective.

A third means provides a semiconductor memory device, wherein all spare memory cells are arranged in one of the memory cell blocks. Therefore, this simplifies the organization of semiconductor memory devices.

A fourth mean provide a semiconductor memory device, wherein the spare memory cell is connected to the primary memory cell in the same memory cell block with a shared decode line and is driven through a shared word line drive signal generation circuit. Therefore, the area of a memory chip required can be reduced since the sharing of the word line drive signal generating circuit between the spare word line and the primary word line makes it possible to eliminate a need for the separate provision of such a circuit for both spare and primary word lines.

A fifth means provides a semiconductor memory device further including a decoder that individually drives word lines of the memory cells of each memory cell block; a redundancy-use decision circuit that stores in advance the address of a defective memory cell and outputs a redundancy-use signal if the address of an address signal agrees with the stored address; a predecoder that is responsive to an address signal and sends out a predecode signal to select a word line of the primary memory cell corresponding to the address of the address signal; and a decode signal selection circuit that connects a predecode signal, supplied from the predecoder, to the decoder of the memory cell block containing the primary memory cell corresponding to the address of the address signal while, when a redundancy-use signal is sent out from the redundancy-use decision circuit, connecting the redundancy-use signal to the decoder of the memory cell block containing therein a spare memory cell to be replaced. Therefore, this assures the smooth operation of the decoders of the memory cell blocks.

A sixth means provides a semiconductor memory cell device, wherein: the plurality of memory cell blocks are divided into two block groups; the spare memory cells are arranged in any one of the memory cell blocks of the two block group; if a primary memory cell of one of the two block groups is a defective memory cell, a spare memory cell of the other block group is previously assigned for replacement; and the decode signal selection circuit connects predecode signals to the decoders of one of the block groups which contains the primary memory cell corresponding to the address of the address signal, while connecting redundancy-use signals to the decoders of the other block group which contains the primary memory cell not corresponding to the address of the address signal. Therefore, even if word lines of both the primary and spare memory cells are selected, it is possible to access read data in a nondestructive manner to achieve a high-speed word line activation, an improved defective memory cell corrective efficiency, and an improved post-corrective yield.

A seventh means provides a semiconductor memory device further including a redundancy encoder that encodes a redundancy-use signal fed from the redundancy-use decision circuit to send out a redundancy decode signal to select a word line of a spare memory cell. Therefore, the number of signal lines used to decode a spare memory cell can be decreased even if many spare memory cells are provided, since on the way the output of the redundancy-use decision circuit is encoded by the redundancy encoder.

An eighth means provides a semiconductor memory device, the memory cell blocks are serially arranged and are divided into two block groups by a boundary defined between the two centrally located memory cell blocks; and the memory cell block containing the spare memory cells is positioned at the center. Therefore, this realizes a semiconductor memory device that has a long data hold time and a tougher noise-resistance since a memory cell block with a longer bit line length is arranged inside (for instance, arranged around the center of a memory chip where the variation in memory cell processing is less likely to appear compared to the outside).

A ninth means provides a semiconductor memory device, further including a sense amplifier that is shared between the adjoining memory cell blocks; and switching means for switching signal connection between the sense amplifier and the memory cell blocks at each sides of the sense amplifier. Therefore, the pitch of sense amplifiers can be reduced and the number of sense amplifiers can be reduced thereby greatly reducing the area of the chip.

A tenth means provides a semiconductor memory device further including stop signal output means that sends out, upon receiving a redundancy-use signal from the redundancy-use decision circuit, a primary memory stop signal to the decoder of a defective primary memory cell to stop its operation. Therefore, this eliminates a need for current used to get the primary word line activated thereby achieving lower power consumption.

An eleventh means provides a semiconductor memory device with a plurality of primary memory cells and a plurality of spare memory cells, the semiconductor memory device comprising: a decoder that is so configurated that the primary memory cell and the spare memory cell are interconnected by a shared decode line and driven through a shared word line drive signal generating circuit; and memory replacement means that stores in advance the address of a defective memory cell of the plurality of primary memory cells and makes, when the address of an address signal supplied agrees with the address of the defective memory cell, the decoder operate to select a spare memory cell for the defective primary memory cell. Therefore, this eliminates a need for the separate provision of a word line drive signal generating circuit for both spare and primary word lines.

A twelfth means provide a semiconductor memory cell wherein the memory replacement means includes: a redundancy-use decision circuit that stores in advance the address of a defective memory cell and outputs a redundancy-use signal if the address of an address signal agrees with the stored address; a predecoder that is responsive to an address signal and sends out a predecode signal to select a word line of the primary memory cell corresponding to the address of the address signal; and a decode signal switching circuit that connects a predecode signal, supplied from the predecoder, to the word line drive signal generating circuit, while connecting, when a redundancy-use signal is sent out from the redundancy-use decision circuit, the redundancy-use signal instead of the predecode signal to the word line drive signal generating circuit. Therefore, this makes the switching of selection between a word line of the primary memory cell and another of the spare memory cell smooth since, according to the presence or absence of a redundancy-use signal, the decode signal switching circuit performs switching between the predecode signal and the redundancy-use signal as the input of the drive signal generating circuit.

A thirteenth means provides a semiconductor memory device wherein the number of elements of the redundancy-use decision circuit and the number of decode lines of the word line drive signal generating circuit are even; and the word line drive signal generating circuit is directly decoded by a redundancy-use signal of the redundancy-use decision circuit. Therefore, this reduces the number of devices and wiring thereby reducing the area of the chip.

A fourteenth means provides a semiconductor memory device further including a redundancy encoder that encodes the output of the redundancy-use decision circuit to send out a redundancy decode signal that selects a word line of the spare memory cell. Therefore, it is possible to reduce the amount of wiring to decode the word line of the spare memory cell even if many spare memory cell are provided, since the redundancy-use signal is once translated into the redundancy decode signal that drives the word line of the spare memory cell.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features, and advantages will become more apparent to those skilled in the art from the following description when considered in conjunction with drawings, in which:

FIG. **1** is an electric circuit diagram showing how a semiconductor memory device of a first embodiment of the present invention is organized;

FIG. **2** is an electric circuit diagram of a redundancy encoder of the first embodiment;

FIG. **3** is an electric circuit diagram showing how a predecoder and a decode signal selection circuit of the first embodiment are organized;

FIG. **4** is an electric circuit diagram illustrating how a row decoder of the first embodiment is organized;

FIGS. **5**(*a*) and **5**(*b*) compare a corrective method of the first embodiment with a conventional corrective method;

FIG. **6** is an electric circuit diagram showing how a semiconductor memory device of a second embodiment of the invention is organized;

FIG. **7** is an electric circuit diagram showing how a semiconductor memory device of a third embodiment of the invention is organized;

FIG. **8** is an electric circuit diagram showing how a semiconductor memory device of a fourth embodiment of the invention is organized;

FIG. **9** is an electric circuit diagram showing the organization of a conventional semiconductor memory device;

FIG. **10** is an electric circuit diagram showing the organization of a conventional row decoder; and

FIG. **11** is an electric circuit diagram showing the organization of a conventional semiconductor memory device with plural memory cell blocks.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment I

The first embodiment is now described by making reference to FIGS. **1** to **5**. A semiconductor memory device with a redundant configuration in accordance with this embodiment has a plurality of primary memory cells each of which stores one bit of information, and a plurality of spare memory cells, wherein the whole memory cells are divided into two block groups SA1 and SA2. The block groups SA1 and SA2 are each divided into M memory cell blocks (i.e., 2M memory cell blocks (four memory cell blocks a, b, c, and d in this embodiment)). The memory cell block a (b, c, d) contains a sense amplifier array **1***a* (**1***b*, **1***c*, **1***d*), a primary memory cell array **3***a* (**3***b*, **3***c*, **3***d*), a row decoder **4***a* (**4***b*, **4***c*, **4***d*), and a column decoder **6***a* (**6***b*, **6***c*, **6***d*). In the centrally-located memory cell block b (c), a spare memory cell array **2***b* (**2***c*) is provided which is located next to the primary memory cell array **3***b* (**3***c*), and the row decoder **4***b* (**4***c*) is integrated by connecting the primary memory cell to the spare memory cell with a shared decode line.

Row predecoders **5***l* and **5***r* are provided, which send out PREDECODE SIGNALS **10***l* (for the block group SA1) and **10***r* (for the block group SA2) respectively to select a primary memory cell corresponding to the address of ADDRESS SIGNAL input. Redundancy-use decision circuits **20***l* and **20***r* are provided, which store in advance the addresses of defective primary memory cells in each one of the primary memory cell arrays **3***a* to **3***d* to send out REDUNDANCY-USE SIGNAL if the address of ADDRESS SIGNAL agrees with the address of the defective primary memory cell stored. Redundancy encoders **8***l* and **8***r* are provided, which, upon receiving REDUNDANCY-USE SIGNALS from the redundancy-use decision circuits **20***l* and **20***r*, send out REDUNDANCY DECODE SIGNALS **11***l* and **11***r* to select redundancy memory cells. Further, decode signal selection circuits **9***l* and **9***r* are provided which select either the output of the row predecoders **5***l* and **5***r*, or the output of the redundancy encoders **8***l* and **8***r*.

The redundancy-use decision circuit **20***l* (**20***r*) has elements SDl0 to SDln (elements SDr0 to SDrn), the number of which corresponds to the number of primary memory cells (16 primary memory cells here in this embodiment) to be disposed in the block group SA1 (the block group SA2). For example, the element SDl0 contains fuses the number of which corresponds to the number of addresses of the primary memory cells arranged in the block group SA2. If a defective memory cell is detected during the examination, a corresponding fuse to the address of the defective memory cell is opened up in advance. Therefore, the address of the defective memory cell can be stored.

If ADDRESS SIGNAL Ak is at a "0", this causes the row predecoder **51**, the redundancy-use decision circuit **20***r*, and the redundancy encoder **8***r* to operate. If ADDRESS SIGNAL Ak is at a "1", this causes the row predecoder **5***r*, the redundancy-use decision circuit **201**, and the redundancy encoder **8***l* to operate.

The organization of the redundancy encoder **8** is explained by reference to FIG. **2**. Note that the redundancy encoder **8***l* is organized in basically the same manner that the redundancy encoder **8***r* is organized. As show in the figure, the output of 16 elements SD0 to SD15 of the redundancy-use decision circuit **20** receiving ADDRESS SIGNALS A0 to An are translated into REDUNDANCY DECODE SIGNAL **11** comprised of 4×4 MATRIX SIGNALS RA0 to RA3, RB0 to RB3.

The decode signal selection circuit **9***l* is supplied with PREDECODE SIGNAL **10***l* from the row predecoder **5***l*, and with REDUNDANCY DECODE SIGNAL **11***l* from the redundancy encoder **8***l*. The decode signal selection circuit **9***r*, on the other hand, is supplied with PREDECODE SIGNAL **10***r* from the row predecoder **5***r*, and with REDUNDANCY DECODE SIGNAL **11***r* from the redundancy encoder **8***r*. Then, these PREDECODE SIGNALS **10***l* and **10***r*, fed from the row predecoders **5***l* and **5***r*, are supplied to the row decoders of one of the block groups SA1 and SA2 that contains the primary memory cell whose address corresponds to the input address, while on the other hand, the outputs of the redundancy encoders **8***l* and **8***r*, that is, REDUNDANCY DECODE SIGNALS **11***l* and **11***r* are fed to the row decoders belonging to the other block group that contains no primary memory cell whose address corresponds to the input address. In this embodiment, if ADDRESS SIGNAL Ak is at a "0", the decode signal selection circuit **9***l* supplies the row decoders **4***a* and **4***b* with PREDECODE SIGNAL **10***l* and the decode signal selection circuit **9***r* supplies the row decoders **4***c* and **4***d* with REDUNDANCY DECODE SIGNAL **11***r*. On the other hand, if ADDRESS SIGNAL Ak is at a "1", the decode signal selection circuit **9***l* supplies the row decoders **4***a* and **4***b* with REDUNDANCY DECODE SIGNAL **11***l* and the decode signal selection circuit **9***r* supplies the row decoders **4***c* and **4***d* with PREDECODE SIGNAL **10***r*.

The organization of the row predecoder **5**, together with that of the decode signal selection circuit **9**, is now described with reference to FIG. **3**. Note that the row predecoders **5***l* and **5***r* have basically the same organization, and that the decode signal selection circuits **9***l* and **9***r* have basically the same organization. As shown in FIG. **3**, the row predecoder **5** is made up of three predecoders A, B and C. These predecoders are each provided with four decode lines. The decode lines of the predecoder A are combined with the decode lines receiving REDUNDANCY DECODE SIGNAL **11***l* (MATRIX SIGNALS RA0 to RA3), at each OR gate so that SIGNALS WP0 to WP3 that select primary word lines are sent out. The decode lines of the predecoder B are combined with the decode lines receiving REDUNDANCY DECODE SIGNAL **11***r* (MATRIX SIGNALS RB0 to RB3), at each OR gate so that FIRST GATE VOLTAGE APPLICATION SIGNALS XPA0 to XPA3 are sent out. Through the decode lines of the predecoder C, SECOND GATE VOLTAGE APPLICATION SIGNALS XPB0 to XPB3 are sent out.

Reference is now made to FIG. **4** to describe the organization of the row decoder **4** that is disposed either in the memory cell block b or in the memory cell block c. The row decoder **4** contains a decoder circuit **4***l* in which transistors used to drive the word lines of the primary memory cell array and transistors used to drive the word lines of the spare memory cell array are both arranged in a matrix manner, a word line drive signal generating circuit **21**, comprised of elements WD0 to WD3 that send out DRIVE SIGNALS to the decode circuit **41**, AND gates **193**, and a gate voltage switching circuit **42** that switches, between a "1" and a "0", respective gate voltages of each one of the transistors of the decode circuit **41**. The word lines of the primary memory cell array and the word lines of thee spare memory cell array are connected to the word line drive signal generating circuit **21**, through shared decode lines. With this arrangement, at the time when the redundancy is being selected, decode signal lines WP0 to WP3 are each supplied with REDUNDANCY DECODE SIGNAL, and at the time when the primary word line is being selected, the WP0 to WP3 are each supplied with PREDECODE SIGNAL. This eliminates a need for the separate provision of a redundancy word line drive signal generating circuit and a primary word line drive signal generating circuit (see FIG. **10**).

The operation of a semiconductor memory device having the above-described organization is explained. It is here assumed that a primary word line WLa0 of the memory cell block a contains a defective memory cell, and that the WLa0 is replaced by a spare word line SWc0 of the memory cell block c. An address corresponding to the primary word line WLa0 is pre-stored in the element SDr0 of the redundancy-use decision circuit **20***r*.

ADDRESS SIGNAL (A0 to Ak) corresponding to the primary word line WLa0 is first fed to the row predecoders **5***l* and **5***r* as well as to the redundancy-use decision circuits **20***l* and **20***r*. The row predecoder **5***l* and the decision circuit **20***r* will operate if ADDRESS SIGNAL Ak is at a "0". The addresses of the defective memory cells, which are stored in the elements SDr0 to SDrn of the decision circuit **20**, are individually compared with this ADDRESS SIGNAL. If the address of ADDRESS SIGNAL input corresponds to the

word line WLa0 of the defective memory cell, the element SDr0 of the decision circuit 20 sends out REDUNDANCY SELECTION SIGNAL SWD0. The redundancy encoder 8r sends out SIGNALS RA0 and RB0 as REDUNDANCY DECODE SIGNAL.

The input of the predecoders A to C of the row predecoder 5r becomes a "0". Of REDUNDANCY DECODE SIGNAL 11r only SIGNALS RA0 and RB0 are supplied at a "1". Accordingly, in the decode signal selection circuit 9r, only PREDECODE SIGNAL WP0 and FIRST GATE VOLTAGE APPLICATION SIGNAL XPA0 become a "1". In the row decoder 4r, shown in FIG. 4, a voltage is applied to the element WD0 of the word line drive signal generating circuit 21, and through the AND gates only the spare word lines become a "1", as a whole. From among the spare word lines, a spare word line SWa, which corresponds to the element WD0, is selected.

In the row predecoder 5l and the decode signal selection circuit 91, if ADDRESS SIGNAL Ak is at a "0", the input of the predecoders A to C of the row predecoder 5l becomes a "1". Then the predecoder A sends out, according to the address of the WL0, the predecode signal WP0, the predecoder B sends out FIRST GATE VOLTAGE APPLICATION SIGNAL XAP0, and the predecoder C sends out SECOND GATE VOLTAGE APPLICATION SIGNAL XPB0. In the row decoder 41, the input of the word line drive signal generating circuit 2l becomes a "1" and the output of the leftmost AND gate becomes a "1". Thus, no spare word lines are selected but the primary word line WLa0 is selected. However, if the element SDr0 of the redundancy-use decision circuit 20 sends out REDUNDANCY-USE SIGNAL (i.e., PRIMARY MEMORY STOP SIGNAL 181), no primary memory cells will be accessed since the primary word line drive signal generating circuit 2l is not operating now.

In accordance with the foregoing operation, the spare word line SWc0 is selected if the primary word line WLa0 contains a defective memory cell. In this way, the word line WLa0 where a defective memory cell is existent is replaced by the spare word line SWc0 to correct the defective memory cell.

As described above, this embodiment makes it possible to replace a primary word line, through which a defective memory cell is accessed, with a spare word line in one of memory cell blocks, whereby the defective word line corrective efficiency becomes increasingly improved, which is shown in FIG. 5a (showing prior art) and FIG. 5b (present invention). In both the prior art and the present invention, the number of spare word lines is four. If, in a certain memory chip, the primary word lines WLa0 and WLa1 of the memory cell block a each contain a defective memory cell, the prior art technique of FIG. 5a is able to correct only the WLa0 by replacing it with the spare word line SWa0 but is unable to correct the WLa1 because there are no spare word lines left in the memory cell block a. As a result, this memory chip becomes defective. Conversely, in accordance with the present invention of FIG. 5b, it is possible to replace any primary word line of the memory cell blocks a and b either with the spare word line SWc0 or with the spare word line SWc1. Thus, as shown in the figure, it is possible for the WLa0 to be replaced by the SWc0, and for the WLa1 by the SWc1. Even if a plurality of defective memory cells are found in one memory cell block in a memory chip, such a memory chip is immune from being defective. The corrective efficiency can be improved, accordingly.

If primary word lines and spare word lines are provided in one memory cell block, as in the conventional redundant system, this may cause a double-selection (that is, a primary word line and a spare word line are selected at the same time resulting in destroying read data) unless the spare word line is selected after PRIMARY MEMORY STOP SIGNAL is generated, the row decoder comes to a stop, and the primary word line becomes non-selective. Therefore, the primary word line must be activated after; the completion of redundancy-use decision, and the spare word line must be activated after inhibiting the primary word line. This prolongs access time. In the first embodiment, on the other hand, primary word lines and corresponding spare word lines are provided in different memory cell blocks, so that even if the simultaneous selection of a primary word line and a spare word line takes place, this will not destroy read data. Therefore, the spare word line and the primary word line can be activated, regardless of mutual timing. A high-speed word line activation can be accomplished, accordingly.

In this embodiment, the decode signal selection circuits 9l and 9r are used to feed REDUNDANCY DECODE SIGNAL for selecting the spare word lines SWb0 to SWbn, SWc0 to SWcn to a signal line shared with PREDECODE SIGNAL for selecting the primary word lines WLb1 to WLbm, WLc1 to WLcm. The word line drive signal generating circuit 2l is shared. This therefore eliminates needs for the separate provision of primary decode lines and redundancy decode lines, and for the separate provision of a primary word line drive signal generating circuit and a redundancy;word line drive signal generating circuit. The area of the memory chip can be reduced, in other words, a larger scale integration of semiconductor memory devices can be achieved.

As a means for replacing a defective memory cell with a spare memory cell, the redundancy-use decision circuits 201 and 20r, the row predecoder 5l and 5r, and the decode signal selection circuits 9l and 9r are provided. This allows the row decoders 4a to 4d of the memory cell blocks a to d to operate efficiently, and a word line corresponding to the address of ADDRESS SIGNAL can be driven without increasing the memory chip area.

For a 64-megabit DRAM, for example, if the total numbers of spare word lines per chip are the same, the invention can be expected to roughly have a double improvement in yield over the conventional redundant system. For a 1-gigabit DRAM, the present invention can be expected to have a five-fold improvement in yield as compared with the conventional redundant system.

For a 64-megabit DRAM, the conventional redundancy system, in order to obtain the same yield as the present redundancy system, requires a chip area approximately 5 mm^2 greater than that required by the present redundancy system, and as to a 1-gigabit DRAM, the conventional redundant system requires a chip area about 15 mm^2 greater than that required by the present redundancy system.

The provision of the redundancy encoders 8l and 8r can reduce the number of signal lines for redundancy decode signals. For example, as shown in FIG. 2, only eight redundancy decode lines, used to connect MATRIX SIGNALS RA0 to RA3, RB0 to RB3 to 16 REDUNDANCY-USE SIGNALS, are required.

The first embodiment has been described taking a DRAM with four memory cell blocks as an example, which is not to be considered restrictive. DRAMs, of other types, with a different number of memory cell blocks may be available.

Because of encoding by the redundancy encoders 8l and 8r, even in the organization of the first embodiment, the decode signal selection circuit 9 is used to feed REDUN-

DANCY DECODE SIGNAL for selecting a great number of spare word lines to a signal line shared with PREDECODE SIGNAL to share a word line drive signal generating circuit. This effectively produces a chip area reducing effect.

In the first embodiment, two of the four memory cell blocks located inside contain spare word lines. The variation in memory cell processing is more likely to appear at the outside of a chip than the inside. If a memory cell block with a shorter bit line length including only primary word lines is arranged outside, and a memory cell block with a longer bit line length including spare word line is arranged inside (for instance, arranged around the center of a memory cell array), this realizes a semiconductor memory device that has a long data hold time and a tougher noise-resistance.

As described above, the generation of PRIMARY MEMORY STOP SIGNAL **18** brings the operation of the row decoder **4** to a halt. Therefore, no currents are required for selecting and activating the primary word line WL, resulting in achieving less power consumption. Further, since it is unnecessary to get the primary word line WL activated after redundancy-use decision is completed and PRIMARY MEMORY STOP SIGNAL **18** is established, there are no possibilities of a drop in operation speed.

Embodiment II

The second embodiment is now described. In the first embodiment, if a primary memory cell in one memory cell array is found to be defective, the defective memory cell is replaced by a spare memory cell in the other memory cell array. Which is not to be considered restrictive. A defective primary memory cell may be replaced by a spare memory cell in the same memory cell array, and when all spare memory cells are used up a further defective memory cell may be replaced by a spare memory cell in a different memory cell array.

FIG. **6** shows the organization of a semiconductor memory device in accordance with this embodiment. The memory cell blocks a to d have the primary memory cell arrays **3***a* to **3***d* respectively, and further have the spare memory cell arrays **2***a* to **2***d* respectively. The row predecoder **5**, the redundancy-use decision circuit **20**, comprised of the elements SD0 to SDn, the redundancy encoder **8**, and a memory cell block selection switching circuit **29** are provided.

The operation of the semiconductor memory device of this embodiment is now described. Here, it is assumed that the element SD0 of the redundancy-use decision circuit **20** corresponds to the spare word line SWLa0 of the primary memory cell array **2***a*, and that an address, corresponding to a primary word line containing a defective memory cell, is stored in advance.

If input ADDRESS SIGNAL corresponds to the address of a primary word line containing no defective memory cells, the row predecoder **5** sends out PREDECODE SIGNAL **10** to select such a primary word line together with PRIMARY BLOCK SELECTION SIGNAL **30**. Upon receiving PRIMARY BLOCK SELECTION SIGNAL **30**, the block selection switching circuit **29** sends out BLOCK SELECTION SIGNAL **32**. In this way, the primary word line is selected according to the input address. The redundancy-use decision circuit **20**, on the other hand, sends out no REDUNDANCY-USE SIGNALS, since the stored address of the defective memory cell disagrees with the input address.

When ADDRESS SIGNAL corresponds to the address of a defective memory cell stored in the element SD0 of the decision circuit **20**, the SD0 sends out REDUNDANCY-USE SIGNAL, and REDUNDANCY DECODE SIGNAL **11** to select the spare word line SWLa0 and REDUNDANCY BLOCK SELECTION SIGNAL **31** are supplied from the redundancy encoder **8**. Further, PRIMARY MEMORY STOP SIGNAL **18** is fed to the row decoders **4***a* to **4***d* so that the primary word lines stop operating. Due to the input of PRIMARY MEMORY STOP SIGNAL **18**, the block selection switching circuit **29** translates BLOCK SELECTION SIGNAL **32** from PRIMARY BLOCK SELECTION SIGNAL **30** into REDUNDANCY BLOCK SELECTION SIGNAL **31**. Therefore, no primary word lines are subject to selection, the spare word line SWLa0 is selected, and the sense amplifier and the column decoder of the memory cell block a become activated by REDUNDANCY DECODE SIGNAL **11**.

As described above, in accordance with the second embodiment, BLOCK SELECTION SIGNAL **32** is switched between PRIMARY BLOCK SELECTION SIGNAL **30** and REDUNDANCY BLOCK SELECTION SIGNAL **31** by the output Of the redundancy-use decision circuit **20**. This makes it possible to replace a primary word line of any memory cell block with a spare word line of any memory cell block. For instance, a defective memory cell is replaced by a spare memory cell in the same memory cell block, and when all spare memory cell are used up a further defective memory cell will be replace by a spare memory cell in a different memory cell block. This results in increasingly improving the spare memory cell availability.

Embodiment III

The third embodiment is explained. FIG. **7** shows the organization of a semiconductor memory device according to this embodiment. This semiconductor memory device includes the memory cell blocks a to d, and the sense amplifiers **1***a* to **1***e*, wherein the adjoining memory cell blocks a and b share the sense amplifier **1***b*, the adjoining memory cell blocks b and c share the sense amplifier **1***c*, and the adjoining memory cell blocks c and d share the sense amplifier **1***d*. The memory cell block a (b, c, d) has the primary memory cell array **3***a* (**3***b*, **3***c*, **3***d*). The leftmost and rightmost memory cell blocks a and d have the spare memory cell arrays **2***a* and **2***d* respectively. Further, the leftmost memory cell block a has the row decoder **4***a* that connects the primary memory cell array **3***a* to the spare memory cell array **2***a* with a shared decode line. Likewise, the rightmost memory cell block d has the row decoder **4***d* in which the primary memory cell array **3***d* and the spare memory cell array **2***d* are interconnected by a shared decode line. The central memory cell blocks b and c have the row decoders **4***b* and **4***c* respectively which decode the primary memory cell arrays **3***b* and **3***c* respectively.

Intervened between each one of the sense amplifiers **1***a* to **1***e* and each one of the memory cell arrays of the memory cell blocks a to d are block selection switch arrays **12***al* to **12***dr*. If a primary word line, contained in the primary memory cell array **3***b*, is selected, selection switches of the block selection switch arrays **12***al* and **12***br* are turned on, and switches of the block selection switch arrays **12***ar* and **12***cl* are turned off. At the same time, selection switches of the block selection switch arrays **12***dl* and **12***dr*, of the primary memory cell array **3***d* containing a spare word line corresponding to the selected memory cell block, are turned on, and switches of the block selection switch array **12***cr* are turned off. Other arrangements are the same as the first embodiment (see FIG. **1**).

As seen from the above description, this embodiment can achieve the same remedy efficiency as the first embodiment. Additionally, the pitch of the sense amplifiers **1***a* to **1***e* can be reduced, and the number of sense amplifiers can be decreased. This results in a higher density of semiconductor memory devices per chip.

Embodiment IV

The fourth embodiment is described making reference to FIG. **8**. In this embodiment, both the spare memory cell array **2** and the primary memory cell array **3** are arranged in a single memory cell block, wherein the spare memory cell array **2** and the primary memory cell array **3** are connected by a shared decode line in the row decoder **4**. The row decoder **4** contains the decode circuit **41** in which transistors used to drive the word lines of the primary memory cell array and transistors used to drive the word lines of the spare memory cell array are arranged in a matrix manner, the word line drive signal generating circuit **21**, comprised of the elements WD0 to WD3 that send out DRIVE SIGNALS to the decode circuit **41**, the AND gates, and the gate voltage switching circuit **42** that switches the respective gate voltages of each one of the primary word line drive transistors of the decode circuit **41**, between a "1" and a "0". In other words, the word line of the primary memory cell array and the word line of the spare memory cell array are connected to the word line drive signal generating circuit **21**, through a shared decode line.

In the semiconductor memory device of this embodiment, the row predecoder **5** to send out PRECODE SIGNAL **10** upon receiving ADDRESS SIGNAL, a decode signal switching circuit **19**, and the redundancy-use decision circuit **20** comprised of the elements SD0 to SD3 are arranged. The decode signal switching circuit **19** is supplied with the outputs of the elements SD0 to SD3, and is made up of a stop signal output section **191**, comprised of OR elements to send out PRIMARY MEMORY STOP SIGNAL **18** depending upon the operation of the elements SD0 to SD3 of the redundancy-use decision circuit **20**, an inverter **192** to invert STOP SIGNAL **18** from the stop signal output section **191**, an AND gate **193**, comprised of four AND elements that are supplied with the output of the inverter **192** and with PREDECODE SIGNAL **10** fed from the row predecoder **5**, and an OR gate **194**, comprised of four OR elements that are supplied with the outputs of the elements SD0 to SD3 respectively. The output sides of the OR elements of the OR gate **194** are connected through the predecode lines WP0 to WP3 to the elements WD0 to WD3 of the word line drive signal generating circuit **21**. Further, the output side of the stop signal output section **191** is connected directly to the gates of the spare word line drive transistors of the decode circuit **41** of the row decoder **4**, and is also connected to the gates of the primary word line drive transistors, not directly but through inverters of the gate voltage switching circuit **42**.

The operation of the semiconductor memory device described above is explained. The addresses of primary word lines containing defective memory cells are pre-stored in the elements SD0 to SD3 of the redundancy-use decision circuit **20**.

If an address, which corresponds to a primary word line containing no defective memory cells, is supplied, the row predecoder **5** sends out PREDECODE SIGNAL **10** corresponding to the primary word line thus selected. Since the elements SD0 to SD3 do not send out signals at all if the input address disagrees with the stored address in these elements, the stop signal output section **191** sends out no PRIMARY MEMORY STOP SIGNAL **18**. Therefore, the output of the inverter **192** becomes a "1". In the AND gate **193**, only the AND elements that are supplied with PREDECODE SIGNAL **10** become a "1". The predecode lines WP0 to WP3 are supplied with PREDECODE SIGNAL **10** corresponding to the primary word line at the input address. Correspondingly, the elements WD0 to WD3 of the word line drive signal generating circuit **21** send out WORD LINE DRIVE SIGNAL. Meanwhile, since PRIMARY MEMORY STOP SIGNAL **18** is not fed from the stop signal output section **191**, the gate voltages of the spare word line drive transistors each come to a "0" state. Thus, no spare word lines are selected. Of the outputs of the gate voltage switching circuit **42** the output of the AND gate **193**, connected to a memory cell array at which the primary memory cell corresponding to PREDECODE SIGNAL **10** is placed, becomes a "1". Accordingly, the primary word line, which corresponds to ADDRESS SIGNAL input, is selected.

Next, the operation, at the time when a corresponding address to the address of a defective memory cell stored in the element SD0 of the redundancy-use decision circuit **20** is supplied, is now described. If an input address corresponds to the stored address of the element SD0, this causes the SD0 to send out REDUNDANCY-USE SIGNAL thereby causing the stop signal output section **191** to send out PRIMARY MEMORY STOP SIGNAL **18**. All outputs from the gate voltage switching circuit **42** of the row decoder **4** become a "0", whereby no primary word lines are selected. Due to this PRIMARY MEMORY STOP SIGNAL **18**, the AND gate **193** will not send out PREDECODE SIGNAL **10** but REDUNDANCY-USE SIGNAL, received from the element SD0 of the redundancy-use decision circuit **20**, to the predecode line WP0. Because of PRIMARY MEMORY STOP SIGNAL **18** output from the stop signal output section **191**, the gate voltages of the transistors connected to the word lines of the spare memory cell array **2** become a "1". This results in selecting the spare word line SWL0.

As described above, in this embodiment, the spare memory cell array **2** and the primary memory cell **3** are connected together with a shared decode line. This eliminates a need to provide a dedicated drive signal generating circuit for the spare word lines. The increase of the area of the memory chip due to the arrangement of spare memory cells can be avoided.

Additionally, in this embodiment, the number of elements of the redundancy-use decision circuit **20** and the number of decode lines of the word line drive signal generating circuit **21** are set even, so that the elements WD0 to WD3 of the circuit **21** can directly be selected by REDUNDANCY-USE SIGNALS from the elements SD0 to SD3 of the circuit **20**. This advantageously simplifies the configuration for decoding a spare memory cell corresponding to the address of a defective memory cell.

However, if the decode lines of the word line drive signal generating circuit **21** is outnumbered by the elements of the redundancy-use decision circuit **20**, a redundancy encoder should be provided (see FIG. 1) for translation to a matrix signal. In this case, a great number of spare memory cells can advantageously be arranged.

It is understood that various other modification to the above-described device will become evident to those skilled in the art. For that reason the arrangement described herein is for illustrative purposes only and is not to be considered restrictive.

The invention claimed is:

1. A semiconductor memory device with a plurality of primary memory cells and a plurality of spare memory cells, the semiconductor memory device comprising:

decoder means for interconnecting the primary memory cell and the spare memory cell through a shared decode line which is driven through a shared word line drive signal generating circuit; and

memory replacement means coupled to said decoder means for storing in advance an address of a defective memory cell of the plurality of primary memory cells and makes, when an address signal corresponding to a memory cell to be accessed agrees with the address of the defective memory cell, the decoder means operates to select the spare memory cell to replace the defective primary memory cell.

2. A semiconductor memory device as in claim 1, wherein the memory replacement means includes:

a redundancy-use decision circuit that stores in advance the address of said defective memory cell and outputs a redundancy-use signal if the address signal agrees with the stored address;

a predecoder responsive to the address signal and sends out a predecode signal to select a word line of the primary memory cell corresponding to the address signal; and

a decode signal switching circuit that connects the predecode signal, supplied from the predecoder, to the word line drive signal generating circuit, while on the other hand connecting, when said redundancy-use signal is sent out from the redundancy-use decision circuit, the redundancy-use signal instead of the predecode signal to the word line drive signal generating circuit.

3. A semiconductor memory device as in claim 2, further including:

a redundancy encoder that encodes the output of the redundancy-use decision circuit to send out a redundancy decode signal to select a word line of said spare memory cell.

4. A semiconductor memory device comprising:

a plurality of memory cell blocks each containing a plurality of memory cells, wherein a fraction of the memory cells of at least one of said memory cell blocks function as primary memory cells and the remaining memory cells function as spare memory cells,

decoder means for accessing word lines of said primary and said spare memory cells of said at least one of said memory cell blocks, said decoder means comprising a plurality of decode lines for supplying a drive signal to said word lines of said primary and said spare memory cells, said word lines of said primary memory cells and spare memory cells are connected by a plurality of shared decode lines and are driven through a shared word line drive signal generation circuit, and

memory replacement means for controlling said decoder means such that when a requested memory cell address corresponds to a defective primary memory cell the decoder means operates to select a spare memory cell selected to replace said defective primary memory cell, wherein said spare memory cell is defined to be select able from a memory cell block other than the memory cell block containing said defective primary memory cell.

5. A semiconductor memory device as in claim 4, further including:

a decoder that individually drives word lines of the memory cells of each memory cell block;

a redundancy-use decision circuit that stores in advance the address of the defective primary memory cell and outputs a redundancy-use signal when an address signal corresponding to a memory cell to be accessed agrees with the stored address;

a predecoder responsive to the address signal and sends out a predecode signal to select a word line of the primary memory cell corresponding to the address signal; and

a decode signal selection circuit that connects the predecode signal, supplied from the predecoder, to the decoder of the memory cell block containing the primary memory cell corresponding to the address signal while, when said redundancy-use signal is sent out from the redundancy-use decision circuit, connecting the redundancy-use signal to the decoder of the memory cell block containing therein said spare memory cell.

6. A semiconductor memory device as in claim 5, wherein:

the plurality of memory cell blocks are divided into two block groups;

the spare memory cells are arranged in any one of the memory cell blocks of the two block groups;

if a primary memory cell of one of the two block groups is a defective memory cell, a spare memory cell of the other block group is previously assigned for replacement; and

the decode signal selection circuit connects predecode signals to the decoders of one of the block groups which contains the primary memory cell corresponding to the address signal, while connecting redundancy use signals to the decoders of the other block group which contains the primary memory cell not corresponding to the address signal.

7. A semiconductor memory device as in claim 5, further including a redundancy encoder that encodes said redundancy-use signal fed from the redundancy-use decision circuit to send out a redundancy decode signal to select a word line of said spare memory cell.

8. A semiconductor memory device as in claim 5, further including:

stop signal output means that sends out, upon receiving said redundancy-use signal from the redundancy-use decision circuit, a primary memory cell stop signal to the decoder of said defective primary memory cell to stop the operation of the defective primary memory cell.

9. A semiconductor memory device as in claim 6, wherein:

the memory cell blocks are arranged in a row and are divided into two block groups by a boundary defined between the two centrally located memory cell blocks; and

the memory cell block containing the spare memory cells is positioned at the center.

* * * * *

FIG. 1

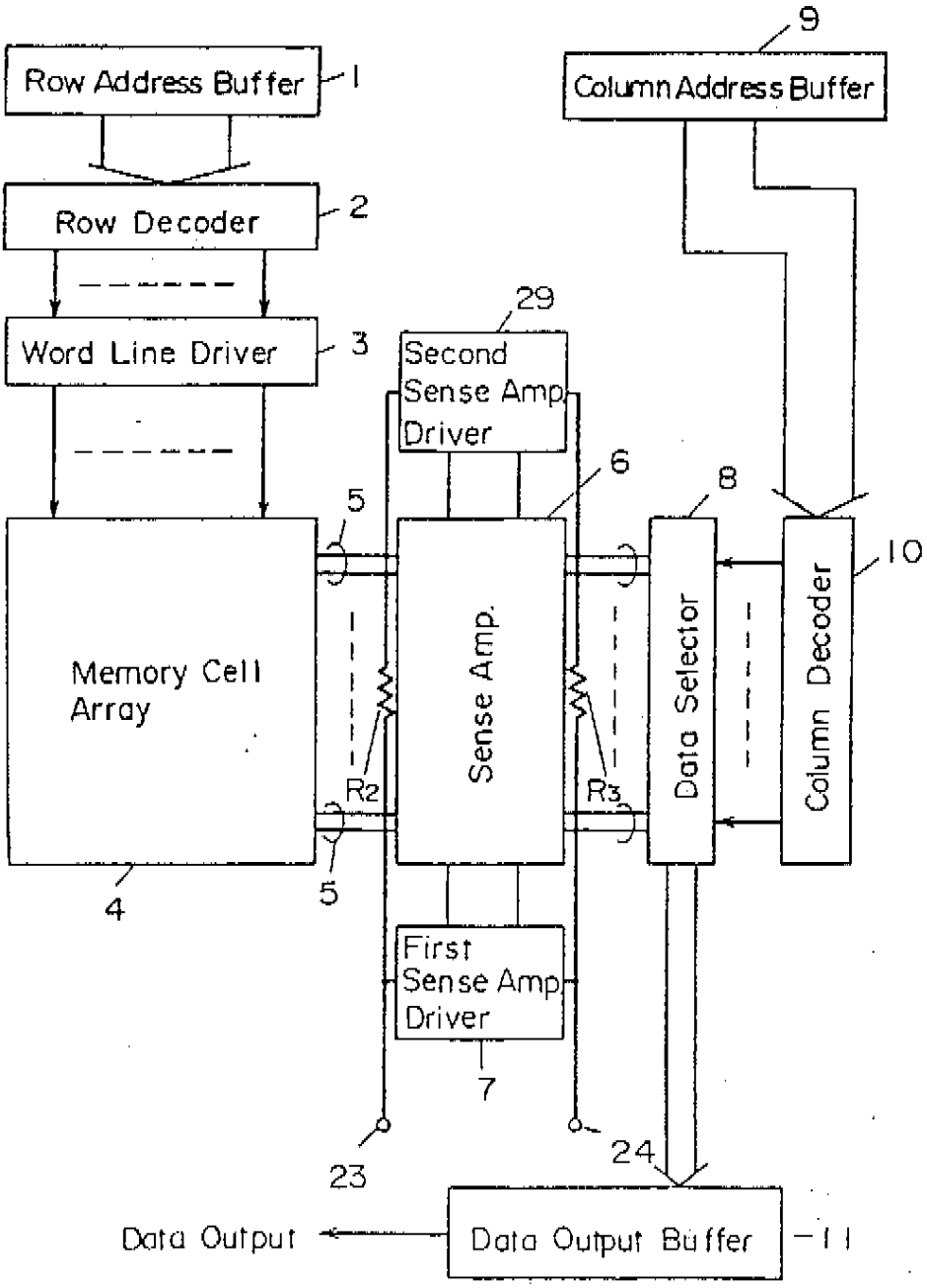

Row Address Buffer
1
Column Address Buffer
9
Row Decoder
2
Word Line Driver
3
29
Second Sense Amp Driver
6
8
5
10
Memory Cell Array
Sense Amp.
Data Selector
Column Decoder
R2
R3
4
5
First Sense Amp Driver
7
23
24
Data Output
Data Output Buffer
11

FIG. 2

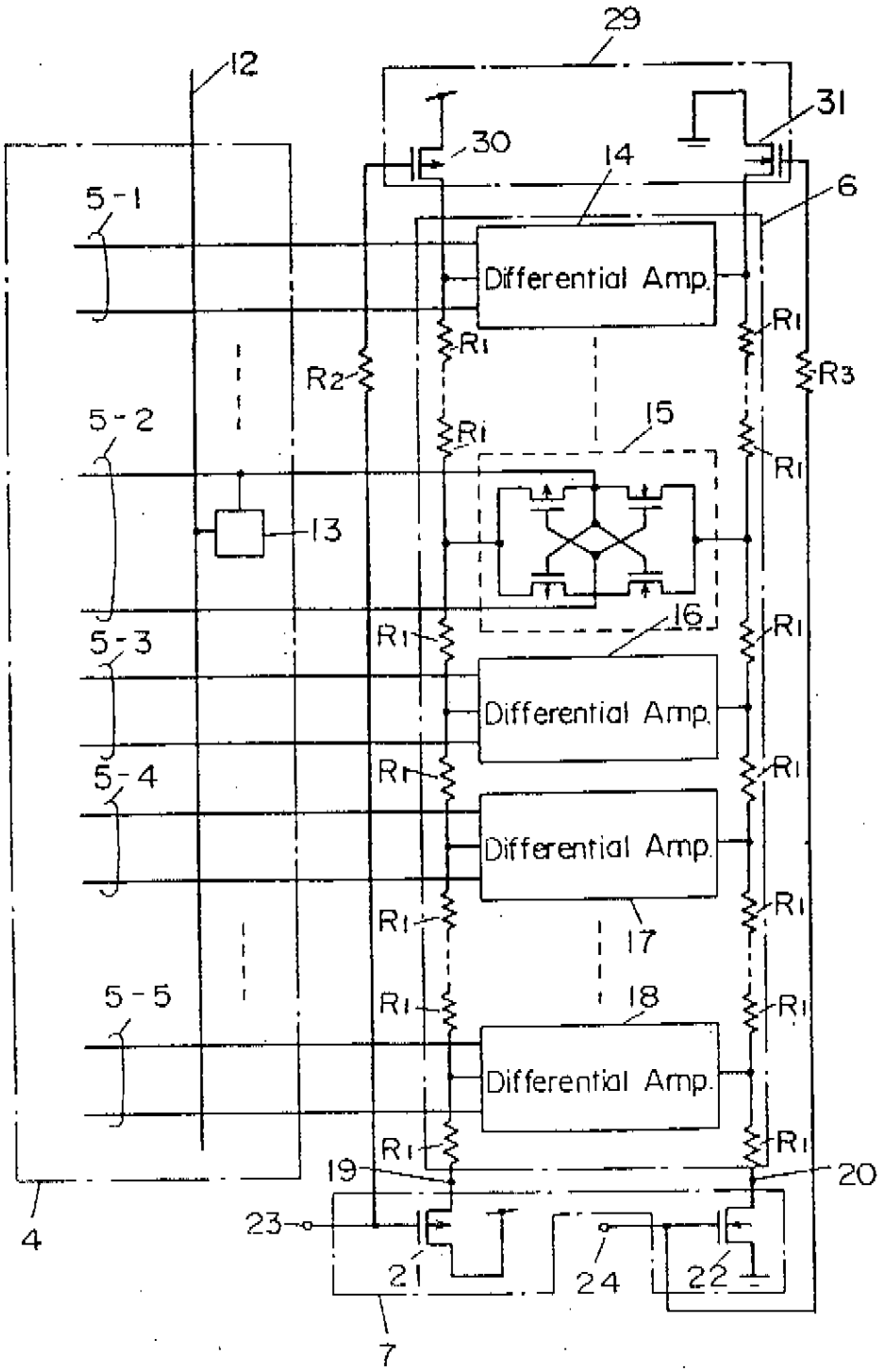

29
12
31
30
14
6
5-1
Differential Amp.
R1
R3
R2
5-2
15
13
16
5-3
Differential Amp.
5-4
Differential Amp.
17
5-5
18
Differential Amp.
19
20
23
21
24
22
4
7

FIG. 3

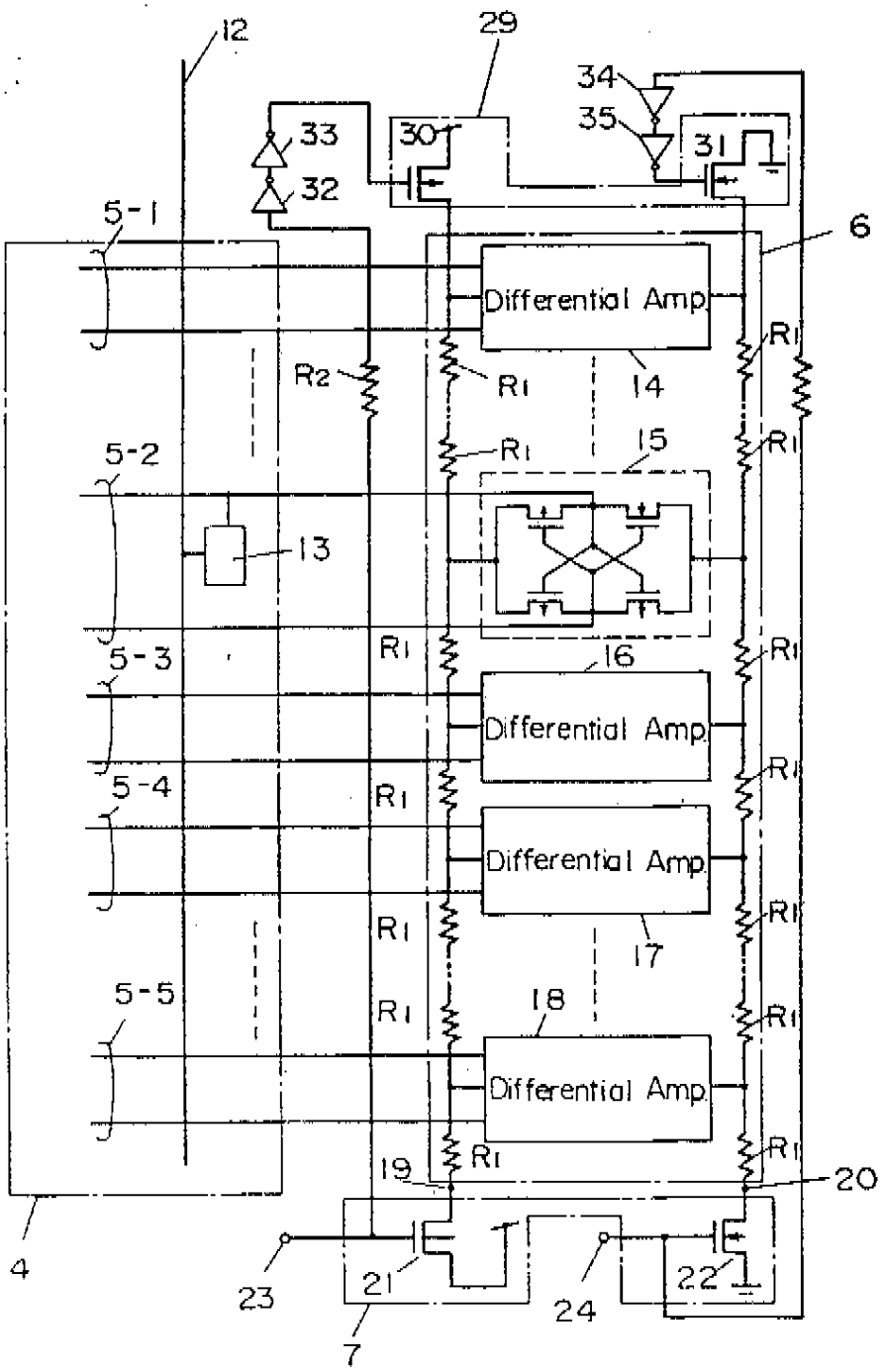

12
29
34
35
33
32
30
31
5-1
6
Differential Amp
R1
R2
14
5-2
15
13
5-3
16
5-4
17
5-5
18
19
20
4
23
21
24
22
7

FIG. 4

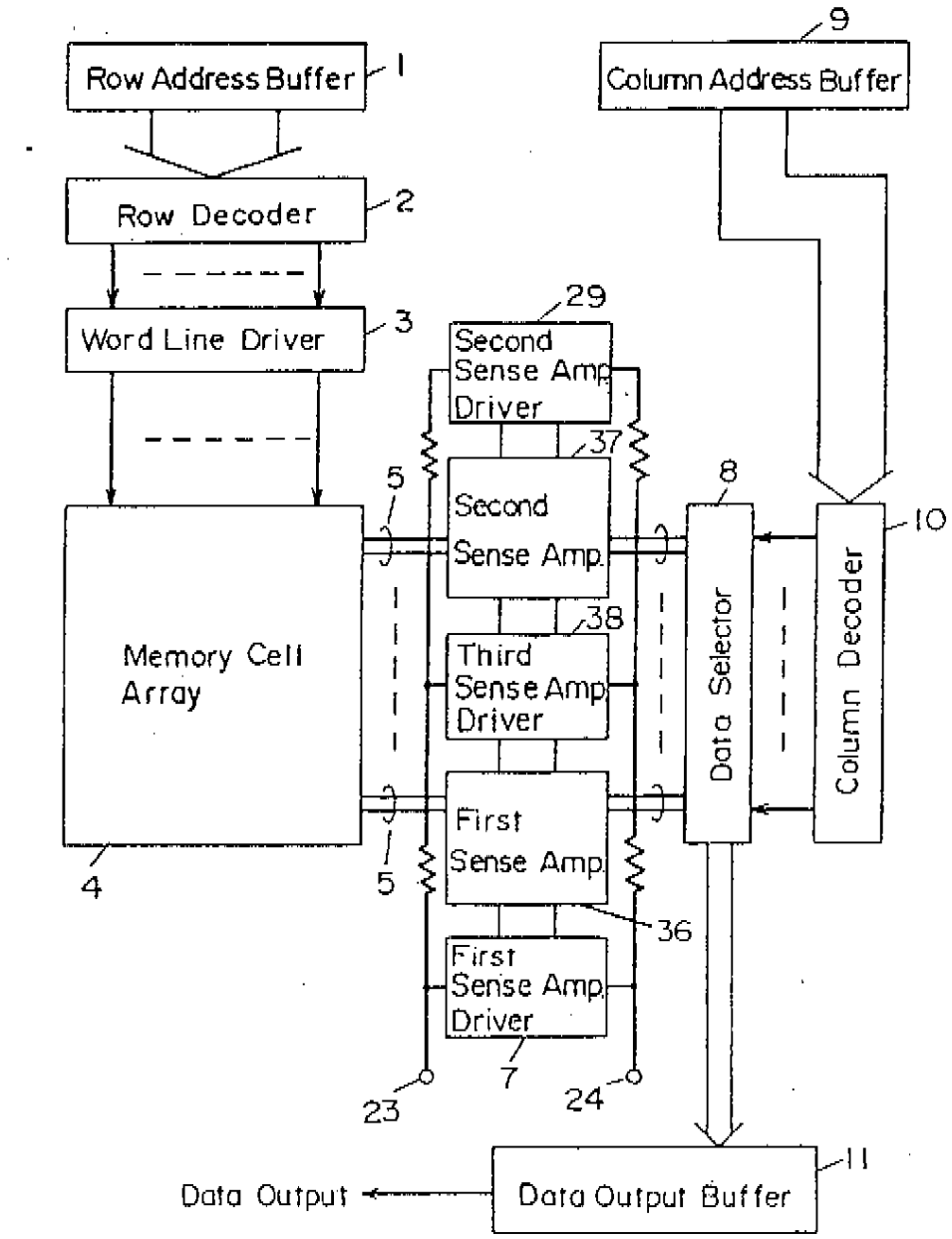

Row Address Buffer
1
Column Address Buffer
9
Row Decoder
2
Word Line Driver
3
29
Second Sense Amp Driver
37
Second Sense Amp
5
8
10
Memory Cell Array
Third Sense Amp Driver
38
Data Selector
Column Decoder
First Sense Amp
4
5
36
First Sense Amp Driver
7
23
24
Data Output
Data Output Buffer
11

FIG. 5

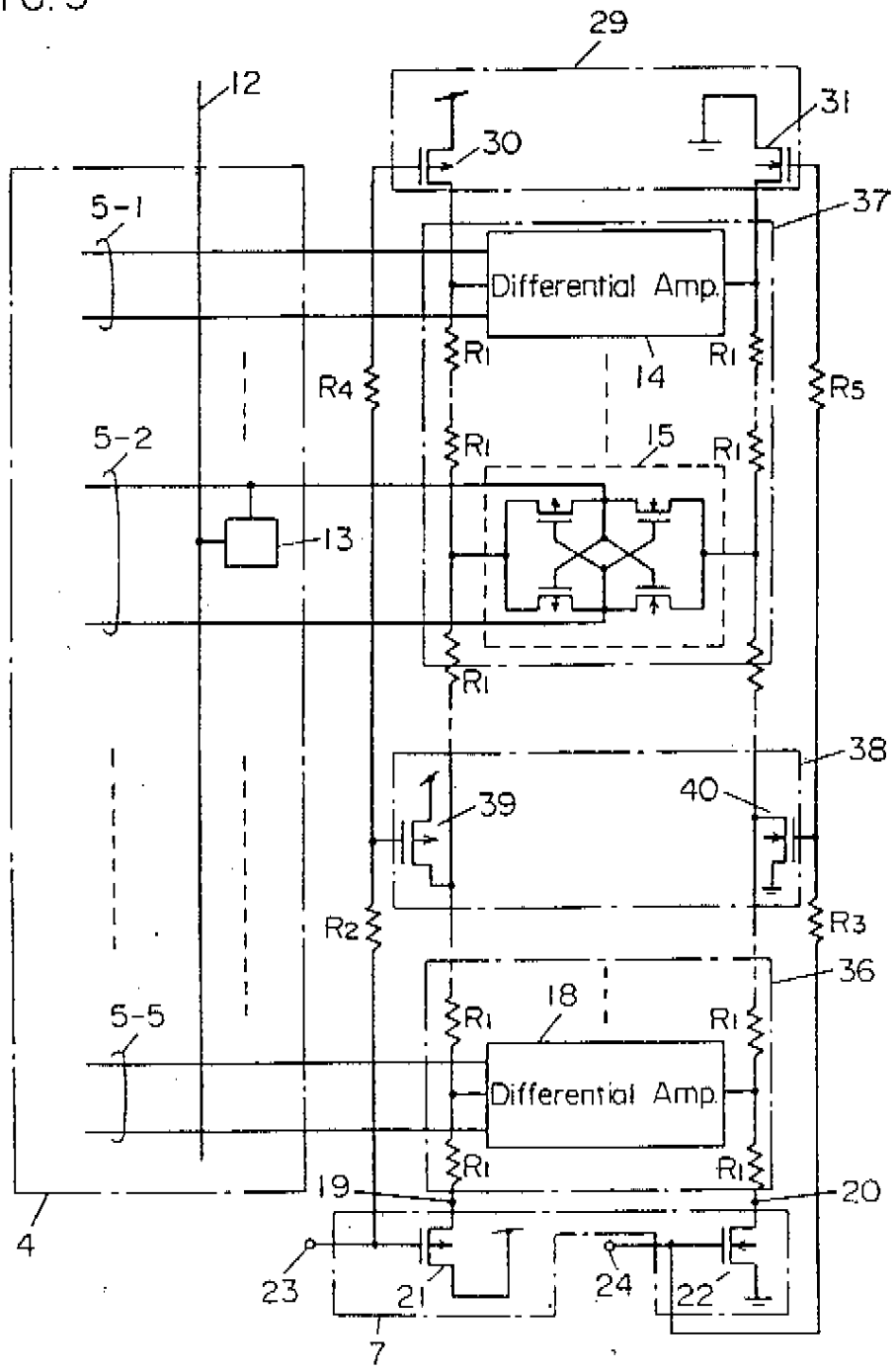

29
12
31
30
37
5-1
Differential Amp.
R1
14
R4
R5
5-2
15
13
38
39
40
R2
R3
36
18
5-5
Differential Amp.
19
20
4
23
21
24
22
7

FIG. 6 PRIOR ART

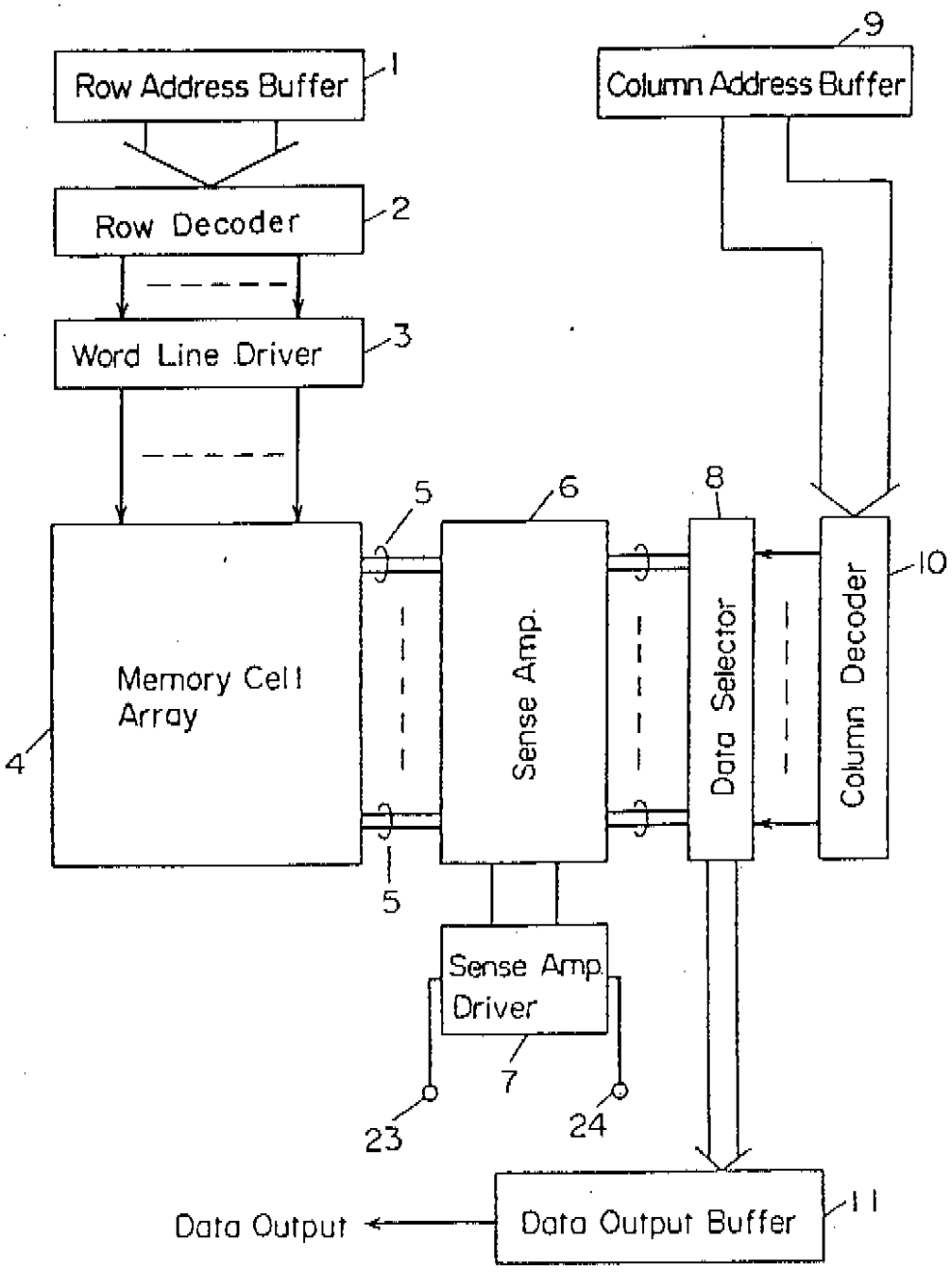


FIG. 7 PRIOR ART

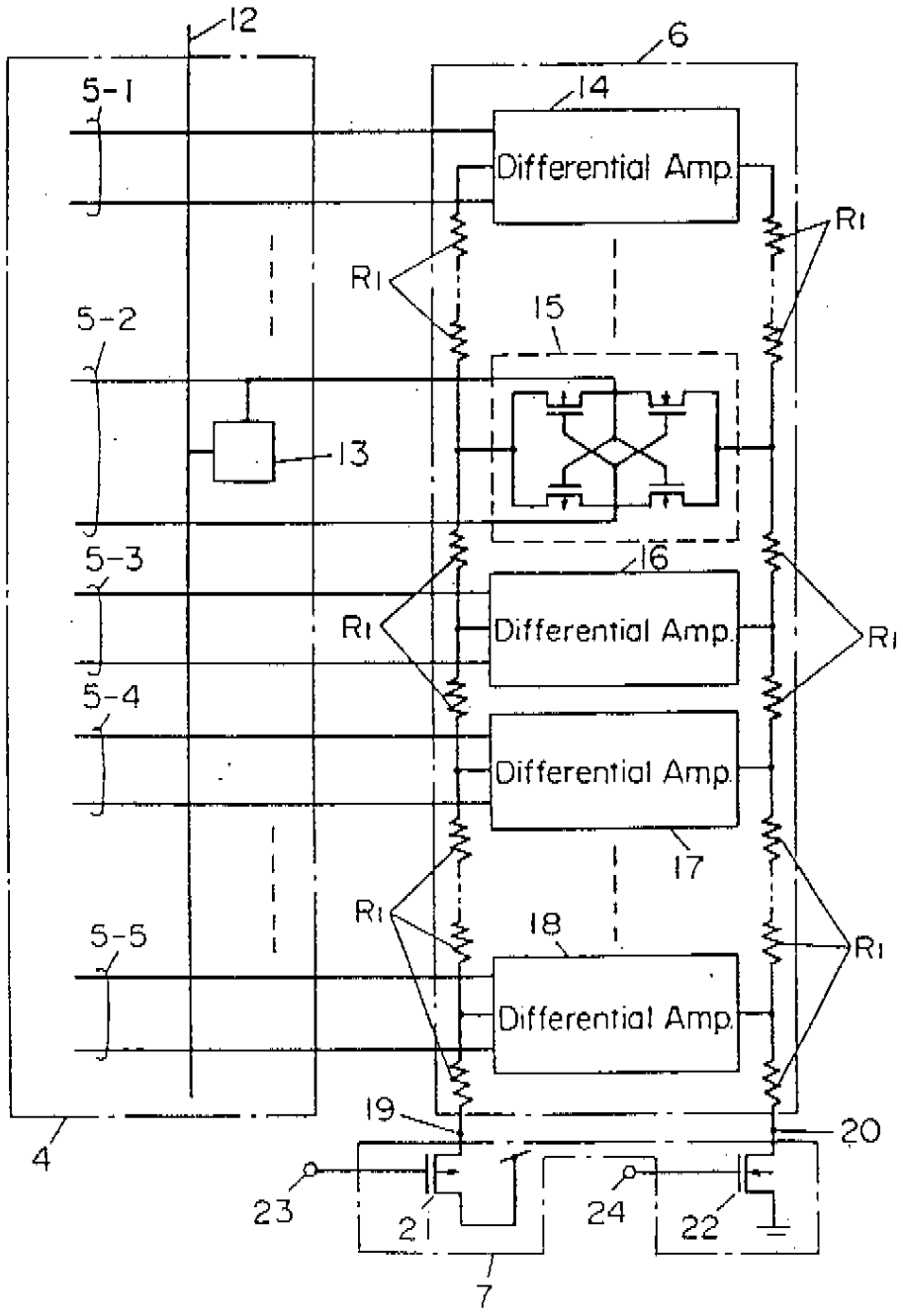


FIG. 8 PRIOR ART

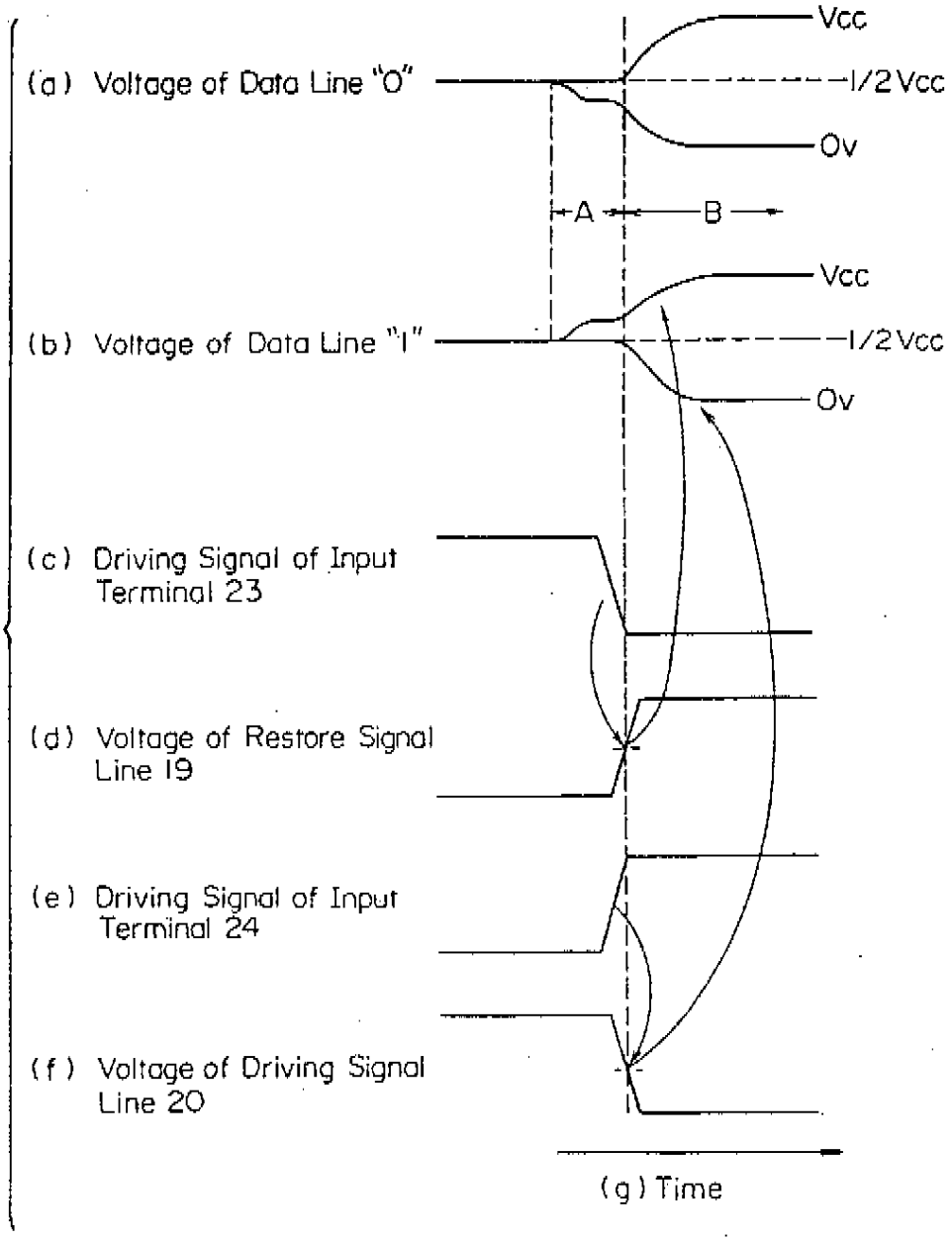
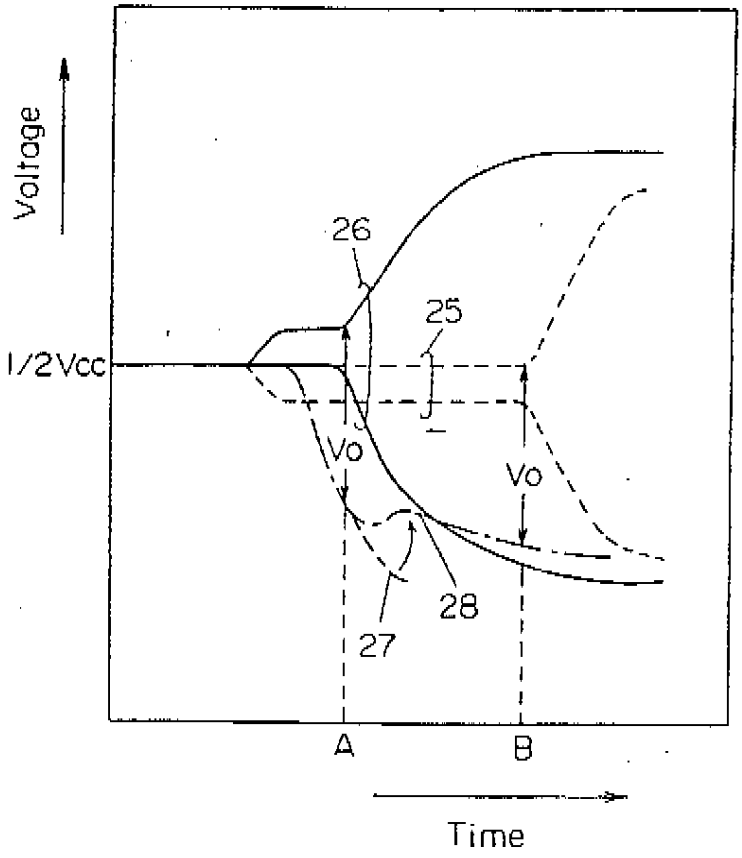


FIG. 9 PRIOR ART



SEMICONDUCTOR MEMORY DEVICE WITH DUAL DRIVERS TO SENSE AMP ARRAY

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor memory device in which a capacity element is used as a memory cell.

Recently, the integration of a semiconductor memory device has increased, and accordingly, the semiconductor memory device, which results in subsequent chip size of the semiconductor memory device has increased. Such an increase in chip size may cause longer wiring lengths, and the wiring resistance may greatly affect the semiconductor memory device in high-speed and stable operations.

FIG. **6** is a block diagram showing a substantial part of a conventional semiconductor memory device.

Referring to FIG. **6**, a description of the data read-out operation follows. A row address signal latched by a row address buffer **1** is decoded by a row decoder **2**. A specific word line in a memory cell array **4** in which a number of memory cells are arranged in the shape of a matrix is activated by the output signal of a word line driver **3**.

As a result, data from a plurality of memory cells connected to the activated word line is read out via a plurality of data lines **5** into a sense amplifier **6**. The read-out data is amplified by the sense amplifier **6** which is driven by a sense amplifier driver **7**, and then fed to a data selector **8**. On the other hand, column address signals latched by a column address buffer **9** are decoded by a column decoder **10**. The data fed to the data selector **8** is transmitted to a data output buffer **11** in response to the output of a column decoder **10**, and output data is delivered from the data output buffer **11**.

FIG. **7** is a schematic circuit diagram of part of the memory array **4**, the sense amplifier **6** and the sense amplifier driver **7**. As shown in FIG. **7**, the data lines **5-1–5-5** are constituted by a pair of signal lines respectively, and memory cells **13** consisting of capacity elements are connected between one signal line of the respective data lines **5-1–5-5** and word line **12** (FIG. **7** shows only one memory cell **13**). The sense amplifier **6** is comprised of a plurality of differential amplifiers **14–18** each connected to the data lines **5-1–5-5**. The differential amplifiers **14–18** each have a pair of control terminals, one of which is connected to a restore signal line **19** and another to a drive signal line **20**. R1 designates the resistance of the restore signal line **19** and drive signal line **20**. The restore signal line **19** has one end connected to a p-type field effect transistor **21** and the drive signal line **20** has one end connected to an n-type field effect transistor **22**. The sense amplifier driver **7** is constituted by these transistors **21** and **22**. A drive signal which actuates the sense amplifier **6** is applied to the input terminals **23** and **24** of the sense amplifier driver **7**. The differential amplifiers **14–18** are constituted, as specified by the differential amplifier **15**, by a pair of n-type field effect transistors and a pair of p-type field effect transistors.

FIG. **8** shows voltages waveforms produced in the operation of the conventional semiconductor memory devices as shown in FIGS. **6** and **7**. The abscissa axis represents time. The change of potential of the data lines **5-1–5-5** connected to the differential amplifiers **14–18** can be viewed with respect to the areas A and B in FIG. **8**. The area A shows the change of potential

when the data lines **5-1–5-5** are connected to the memory cells **13**. In this area, the differential amplifiers **14–18** do not operate yet. The potentials of the data lines **5-1–5-5** vary with the state (0–1) of the data stored in the memory cells **13**. If the data is "0", the potential of one signal line of the pair of data lines will become negative with respect to a half potential of a source voltage Vcc. If the data is "1", the potential will be positive. The area B shows the potential change after the differential amplifiers **14–18** have operated. In the area B, the voltage at the input terminal **24** of the sense amplifier driver **7** rises from the ground level, and the transistor **22** turns on. As a result, the drive signal line **20** will be grounded, so that all the differential amplifiers **14–18** will operate. Consequently, the potential of the lower voltage signal line of each pair of data lines is pulled down to the ground level. On the other hand, the voltage level at the input terminal **23** of the sense amplifier driver **7** will reach the ground level, and the transistor **21** turns on. Consequently, the potential of the higher voltage signal line of each pair of data lines is pulled up to the source voltage Vcc.

With such a conventional semiconductor memory device, however, there lies a problem in that high speed and stable operation can not be expected when the chip size becomes large due to the increase in the number of memory cells and the resultant increase in the length of the wiring.

FIG. **9** shows the potential change under the condition that only one of the differential amplifiers **14–18** amplifies the data "0" and all the rest differential amplifiers amplify the data "1". In FIG. **9**, **25** identifies a potential change of the data line when the data "0" is read out, and **26** is a potential change of the data line when the data "1" is read-out. Elements **27** and **28** are a potential change of the drive signal line **20**; it is shown that the wiring resistance R1 has a small value at **27** and that the wiring resistance R1 has a great value at **28**.

As is apparent from curves **25** and **26** in FIG. **9**, before operating the differential amplifiers **14–18**, the potential of the data line of data "1" rises rapidly, while the potential of the data line of data "0" rises slowly. The differential amplifiers **14–18** start their operation when the potential of drive signal line **20** drops to the value which the potential difference between the higher voltage signal line of a pair of data lines and the drive signal line **20** becomes equal to a threshold voltage Vo. In FIG. **9**, the differential amplifier starts amplification of data "1" at the time A. At this time, the wiring resistance R1 of the drive signal line **20** is small, the differential amplifier instantly starts amplification of data "0". However, if the wiring resistance R1 is large, all differential amplifiers **14–18** operate simultaneously, and thus, a great deal of instantaneous electrical current flows. This causes a potential drop at the drive signal line **20**, so that there will be a timing delay in the lowering of a drive signal as shown by the curve **28** despite the fact that there should be an inherent variation as shown by the curve **27**. As a result, the operation start timing of the differential amplifiers for amplifying the data at state "0" moves from the point A to the point B. If such a delay increases, it becomes difficult to transmit the data correctly to a following circuit.

The pair of n-type field effect transistors perform operations dominantly in the differential amplifiers **14–18** as shown in FIG. **7**. Thus, as in FIG. **9**, when a single differential amplifier serves to amplify the data

"0" and all the remaining differential amplifiers serve to amplify the data "1", a delay of the operation start timing will become significant.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a semiconductor memory device which may overcome the conventional problems.

One object of the present invention is to provide a semiconductor memory device in which the influence of the wiring resistance can be lessened to enable high-speed operation.

Another object of this invention is to provide a semiconductor memory device which makes it possible to reduce the instantaneous current in the operation of the sense amplifier.

In accordance with the present invention, in short, a sense amplifier is driven by two sense amplifier drivers which operate at different from each other.

This can prevent the increase of the peak value of an instantaneous current in the operation of the plurality of differential amplifiers, thus resulting in ensuring that the potential of the signal line connected to the sense amplifiers will be changed in a rapid manner. This may bring about a solution of the problem of the delay in timing of starting of specific differential amplifiers so as to enable correct data to be transmitted to the next circuit at all times.

Further objects and effects of the present invention will become clear by describing the embodiments with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a substantial part of the semiconductor memory device in accordance with the present invention;

FIG. **2** is a schematic circuit diagram of the sense amplifier and its peripheral circuits of FIG. **1**;

FIG. **3** is a schematic circuit diagram of the sense amplifier and its peripheral circuits of the semiconductor memory device of a second embodiment according to the present invention;

FIG. **4** is a block diagram showing a substantial part of the semiconductor memory device of a third embodiment of the present invention;

FIG. **5** is a schematic circuit diagram of the sense amplifiers and its peripheral circuits of FIG. **4**;

FIG. **6** is a block diagram of a substantial part of a conventional semiconductor memory device;

FIG. **7** is a schematic circuit diagram of the sense amplifier and its peripheral circuits of FIG. **6**; and

FIGS. **8** and **9** are views showing voltage waveforms used for the description of the conventional semiconductor memory device.

DETAILED DESCRIPTION OF THE INVENTION

The embodiments of the present invention will now be described with reference to the drawings.

FIG. **1** is a view showing the first embodiment of the present invention. FIG. **1** is different from FIG. **6** only in that the sense amplifier **6** has one end connected to a first sense amplifier driver **7**, and has its other end connected to a second amplifier driver **29**.

FIG. **2** is a view showing a particular circuitry arrangement containing the sense amplifier **6** and its peripheral circuits in FIG. **1**. In FIG. **2**, the same reference numbers are applied to the same elements as those of the prior art as shown in FIG. **7**. A p-type field effect transistor **30** and an n-type field effect transistor **31** are connected to the other end of the sense amplifier **6**, i.e. the other end of a restore signal line **19** and the other end of a drive signal line **20** respectively, said transistors **30** and **31** constituting a second sense amplifier driver **29**. The gates of the transistors **30** and **31** are connected to the input terminals **23** and **24** of the first sense amplifier driver **7** respectively. R2 and R3 designate wiring resistances of the signal lines adapted to actuate the transistors **30** and **31**.

A description of the embodiment as shown in FIGS. **1** and **2** follows.

First, when data from a memory cell **13** is sensed by data lines **5-1–5-5**, there will arise slight potential differences between the signal lines of each pair of data lines **5-1–5-5**. Then, drive signals are applied to the input terminals **23** and **24** of the first sense amplifier driver **7** so as to make the transistors **21** and **22** of the sense amplifier driver **7** conduct. Consequently, electric current flows in the restore signal line **19** and the drive signal line **20**, and thus, the differential amplifiers **14–18** start to operate. The operation as described above is same as in the prior art.

In the embodiment of FIGS. **1** and **2**, however, at the start of the differential amplifiers **14–18** connected in common to the restore signal line **19** and drive signal line **20**, the second sense amplifier driver **29** starts its operation before a great amount of instantaneous current flows. In other words, prior to the drop of a voltage caused by the instantaneous current through the wiring resistance R1, the transistors **30** and **31** consisting the second amplifier driver **29** conduct late by a time constant determined by the wiring resistances R2 and R3 of the signal lines connected to the second sense amplifier **29** and the parasitic capacitances of these signal lines. As a result, it is possible to to reduce the value of the wiring resistance R1 of the restore signal line **19** and drive signal line **20** to something around the half of the value of the prior art. As shown in FIG. **9**, in the period from the rise of the drive signal to the start of operation of the differential amplifiers **14–18**, a period of time is required wherein the differential amplification signal falls by a threshold voltage Vo below the potential of the data line. Consequently, it is unnecessary for the transistors **30** and **31** constituting the second sense amplifier driver **29** to conduct concurrently with the transistors **21** and **22** constituting the first sense amplifier driver **7**. Thus, by taking advantage of the time constant determined by the wiring resistances R2 and R3 and the parasitic capacitance, the actuation of the second sense amplifier driver **29** is delayed so as to be later than the first sense amplifier driver **7**, to ensure that the peak value of the instantaneous current at the time of start of operation of the differential amplifiers **14–18** will be reduced. As a result, the potential of the drive signal line **20** presents a change close to that shown by a curve **27** of FIG. **9**, dropping at a rapid speed. In this connection, the differential amplifiers for amplifying the data "0" can start at the time near the point A rather than removing its starting time to the point B as in the case of the prior art. The precise transmission of data to the next circuit can be secured accordingly.

FIG. **3** is a view showing a circuit of the sense amplifier and its peripheral circuits in the semiconductor memory device of the second embodiment in accordance with the present invention.

In the drawing, the same reference numbers are applied to the same elements as those shown in FIG. 2. FIG. 3 is a different from FIG. 2 in that two pairs of inverter circuits 32 and 33 and 34 and 35 are connected to two signal lines for supplying a drive signal to the second sense amplifier driver 29. Such an addition of the necessary numbers of inverter circuits 32–35 makes it possible to determine the optimum amount of delay time. As a result, a semiconductor memory device can be made which is capable of, in the most effective manner, restraining the peak value of an instantaneous current at the time of starting of the operation of the differential amplifiers 14–18.

FIG. 4 is a view showing a third embodiment of the present invention. The application of the same reference numbers to the same circuit blocks as those of FIG. 1 avoids the necessity of further descriptions thereof. FIG. 4 differs from FIG. 1 in that there are provided two blocks, i.e. first and second sense amplifiers 36 and 37 which correspond to the sense amplifier 6 in FIG. 1, with a third sense amplifier 38 disposed between said first and second sense amplifiers 36 and 37 to connect it to the latter.

FIG. 5 is a view showing the particular circuits as a substantial portion of FIG. 4. The same reference numbers are applied to the same elements as those in FIGS. 2 and 3, and a further description thereof has been omitted. In FIG. 5, the third sense amplifier driver 38 consisting of a p-type field effect transistor 39 and an n-type field effect transistor 40 is disposed between and connected to the first and second sense amplifiers 36 and 37, R4 and R5 identify wiring resistances of the signal lines extending between the second and third sense amplifier drivers 29 and 38. Such an arrangement ensures that the opposite ends of the first sense amplifier 36 will be driven by means of the first and second sense amplifier drivers 7 and 38 and that the second sense amplifier 37 will be driven by means of the third and second sense amplifier drivers 38 and 29. In this instance, with the first sense amplifier 36, the third sense amplifier driver 38 tends to start later than the first sense amplifier driver 7 by a time constant when the time constant is determined by the wiring resistances R2 and R3 and the parasitic capacitance. And in the second sense amplifier 37, the second sense amplifier driver 29 starts to operate later than the third sense amplifier driver 38 by a time constant determined by the wiring resistances R4 and R5 and the parasitic capacitance. Therefore, reduction of the peak value of the instantaneous current at the time of operation of the differential amplifiers 14–18 can possibly by achieved in either sense amplifiers 36 and 37.

Also, provision can, of course, be made for a necessary number of inverter circuits as shown in FIG. 3 which are connected to the drive signal lines of the first, second and third sense amplifier drivers 7, 29, 38 to obtain the optimum amount of delay time.

Furthermore, a sense amplifier may be divided into more than 3 blocks in such a manner that each of sense amplifier drivers will be located between and connected to the respective sense amplifier blocks.

We claim:

1. A semiconductor memory device comprising:
- a memory cell array having a plurality of memory cells arranged in the form of a matrix;
- a means for reading into a plurality of data lines data from a plurality of memory cells connected to a specific word line by activating said specific word line of said memory cell array;
- a sense amplifier consisting of a plurality of differential amplifiers connected to said plurality of data lines respectively for amplifying the data read into said plurality of data lines;
- first and second sense amplifier drivers connected to the opposite ends of a restore signal line and a drive signal line respectively which are in turn connected to said plurality of differential amplifiers of said sense amplifiers, and
- a delay means for giving a time difference to an operation start timing of said first and second sense amplifier drivers.

2. A semiconductor memory device as defined in claim 1, wherein said delay means is constituted by the wiring resistances and parasitic capacitance of the drive signal lines located between and connected to the said first and second sense amplifier drivers.

3. A semiconductor memory device as defined in claim 1, wherein said delay means is constituted by the wiring resistances and parasitic capacitance of the drive signal lines located between and connected to the said first and second sense amplifier drivers, and an inverter circuit means connected to said drive signal line.

4. A semiconductor memory device comprising:
- a memory cell array having a plurality of memory cells arranged in the form of a matrix;
- a means for reading into a plurality of data lines data from a plurality of memory cells connected to a specific word line by activating said specific word line of said memory cell array;
- a first sense amplifier consisting of a plurality of differential amplifiers connected to a specific number of data lines of said plurality of data lines respectively for amplifying data read into said specific number of data lines;
- a second sense amplifier consisting of a plurality of differential amplifiers connected to remaining data lines of said plurality of data lines respectively for amplifying data read into said remaining data lines;
- first and second sense amplifier drivers connected to the opposite ends of the restore signal line and drive signal line which are in turn connected in common to the differential amplifiers of said first and second sense amplifiers;
- a third sense amplifier driver connected to said restore signal line and said drive signal line which are disposed between said first and second sense amplifiers, and
- a delay means for giving a time difference to the starting operation timing of said first, second and third sense amplifier drivers.

5. A semiconductor memory device as defined in claim 4, wherein said delay means is constituted by the wiring resistances and parasitic capacitance of the drive signal lines located between and connected to said first, second and third sense amplifier drivers.

6. A semiconductor memory device as defined in claim 4, wherein said delay means is constituted by the wiring resistances and parasitic capacitance of the drive signal lines disposed between and connected to said first, second and third sense amplifier drivers, and an inverter means connected to said drive signal lines.

7. A semiconductor memory device comprising:
- a memory cell array having a plurality of memory cells arranged in the form of a matrix;